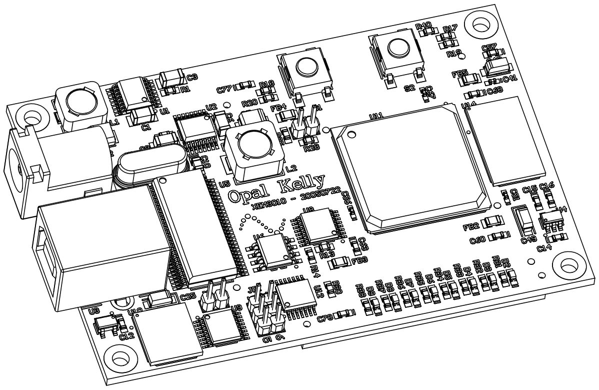
Opal Kelly



XEM3010 User's Manual

A compact (75mm x 50mm) integration board featuring
the Xilinx Spartan-3 FPGA and on-board SDRAM.

The XEM3010 is a compact USB-based FPGA integration board featuring the Xilinx Spartan-3 FPGA, 32 MB 16-bit wide SDRAM, high-efficiency switching power supply, Xilinx configuration PROM, and two high-density 0.8-mm expansion connectors. The USB 2.0 interface provides fast configuration downloads and FPGA-PC communication as well as easy access with our popular FrontPanel software and developer's API. An on-board clock generation device has three independent PLLs and five flexible outputs available to the FPGA, SDRAM, and expansion connectors.

Opal Kelly Incorporated
Portland, Oregon
http://www.opalkelly.com

Revision History:

Date	Description
20051001	Initial release.
20060215	Added reference to Xilinx Answer Record #18095.
20060223	SDRAM clock connection explained.
20060511	Added SDRAM part number.
20060802	Fixed VCCO2/VCCO3 connections table. Added SDRAM to FPGA pin connections.
20070221	Added note about BRK3010 connections.
20070226	Updated host interface pin list.
20070519	Added note regarding heat dissipation.
20070604	Added note about R43 on PCB revision 20070117.
20070613	Removed overline from SDRAM pin names CKE, LDQM, UDQM.
20070919	Made mandatory deassertion of MUXSEL clearer.
20071127	Fixed typo. Pushbuttons are pulled high to 2.5v.

Contents

Introducing the XEM3010

The XEM3010 is a compact (75mm x 50mm, 2.95" x 1.97") FPGA board featuring the Xilinx Spartan-3 FPGA. Designed as a full-featured integration system, the XEM3010 provides access to over 110 I/O pins on its 320-pin Spartan-3 device and has a 32-MByte SDRAM available to the FPGA. The XEM3010 is designed to work with small to medium-sized FPGA designs with a wide variety of external interface requirements.

PCB Footprint

A mechanical drawing of the XEM3010 is shown at the end of this manual. The PCB is 75mm x 50mm with four mounting holes spaced as shown in the figure. These mounting holes are electrically isolated from all signals on the XEM3010. The two connectors (USB and DC power) overhang the PCB by approximately 4mm in order to accomodate mounting within an enclosure.

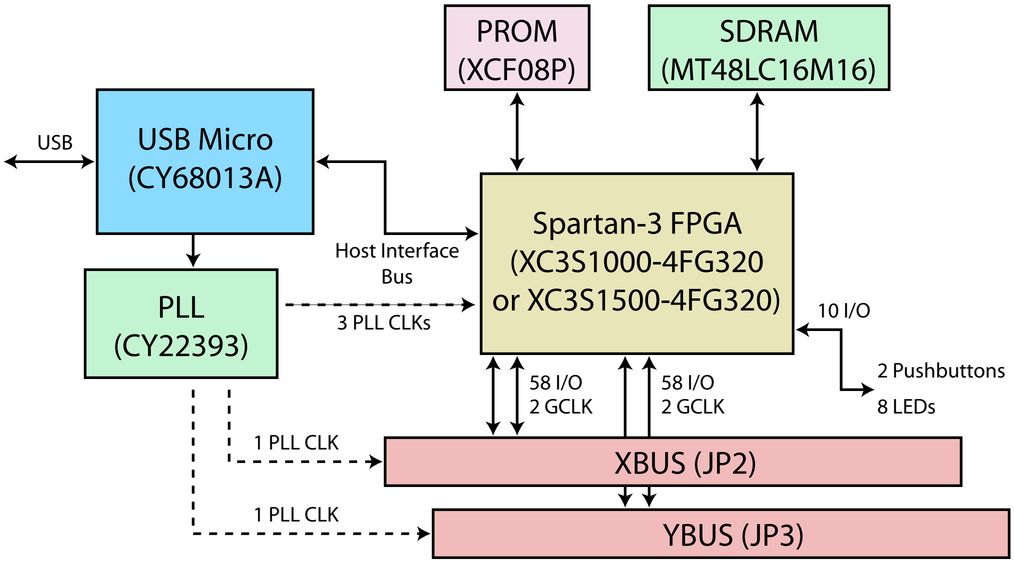
The XEM3010 has two high-density 80-pin connectors on the bottom side which provide access to many FPGA pins, power, JTAG, and the microcontroller's I2C interface.

BRK3010 Breakout Board

A simple breakout board (the BRK3010) is provided as an optional accessory to the XEM3010. This breakout board provides easy access to the high-density connectors on the XEM3010 by routing them to lower-density 0.1"-spaced thru-holes. The breakout board also provides a convenient reference for building boards that will mate to the XEM3010.

A mechanical drawing of the BRK3010 is also shown at the end of this document.

Functional Block Diagram



Power Supply

The XEM3010 is designed to be operated from one of three power sources, depending on user requirements. One of these three sources provides power for the two high-efficiency switching regulators on-board to provide 3.3v and 1.2v. 2.5v and 1.8v are derived from the 3.3v supply using small low-dropout (LDO) regulators.

The three sources and the respective XEM3010 configuration for each are shown in the table below. In all configurations, the XEM3010 requires a clean, well-regulated supply between 4.5v and 5.5v.

Power Source	**XEM3010 Configuration**
DC Power Jack (P1)	No configuration is required. Attach a DC power source to P1 that supplies a clean, regulated voltage of 4.5v to 5.5v.
Expansion Connector (JP3)	No configuration is required. Provide a clean, regulated voltage of 4.5v to 5.5v to the VDC pins on JP3.
USB Bus Power	See section on "USB Bus Power"

IMPORTANT NOTE: Only one power source should be connected at any time. Attaching multiple power sources could damage the XEM3010 and possibly the power source, and void the warranty on the XEM3010.

There two switching regulators on-board, one for the 3.3v supply and one for the 1.2v supply. Each supply has been designed to provide up to 3 A of continuous current. It is unlikely that the XEM3010 will consume this much current, so much of this power will be available to expansion devices using the expansion connectors.

DC Power Connector

The DC power connector on the XEM3010 is part number PJ-102A from CUI, Inc. It has a standard 2.1mm /5.5mm power jack. The outer ring is attached to DGND. The center pin is attached to +VDC on expansion connector JP3 as well as the inputs to the two switching regulators on the XEM3010.

Expansion Bus Power

The expansion bus has pins for +VDC, +3.3V, and +1.2V, making it flexible for nearly any supply scenario. In particular, the following scenarios have been considered:

- +VDC is provided to an expansion device which use or regulate it as necessary.
- +VDC is provided by an expansion device to power the XEM3010.
- +3.3V and/or +1.2V are provided to expansion devices as regulated, reliable supplies.
- +3.3V and/or +1.2V are provided by an expansion device to power the XEM3010. In this case, the switching regulators on the board must be removed. This option may be useful to applications where a switching supply is not desired.

USB Bus Power

The USB 2.0 specification allows for up to 2.5 W (500mA at 5v) to be provided to external peripherals over the USB cable. While power consumption of an unconfigured XEM3010 is quite low, due to the flexibility allowed in FPGA design, the Spartan-3 and SDRAM could easily consume over 2.5 W during operation with a user design, thus violating the USB specification.

However, to support users who may not be consuming that much power in their design and who may still wish to use the XEM3010 in a bus-powered situation, we have provided a solder jumper (J3) on the bottom of the XEM3010. WIth a bead of solder in place across this jumper, the USB +5V is connected to +VDC.

Before relying on USB power, you should be aware of the limitations and the fact that using USB power may render the XEM3010 a USB-noncompliant device.

Supply Heat Dissipation (IMPORTANT!!)

Due to the limited area available on the small form-factor of the XEM3010 and the density of logic provided, heat dissipation may be a concern. This depends entirely on the end application and cannot be predicted in advance by Opal Kelly. Heat sinks may be required on any of the devices on the XEM3010. Of primary focus should be the FPGA (U11), the two switching power supplies (U1, U2), and the SDRAM (U14). Although the two switching supplies are high-efficiency, they are very compact and consume a small amount of PCB area for the current they can provide.

If you plan to put the XEM3010 in an enclosure, be sure to consider heat dissipation in your design.

USB 2.0 Interface

The XEM3010 uses a Cypress CY7C68013A FX2LP USB microcontroller to make the XEM a USB 2.0 peripheral. As a USB peripheral, the XEM is instantly recognized as a plug and play peripheral on millions of PCs. More importantly, FPGA downloads to the XEM happen blazingly fast, virtual instruments under FrontPanel update quickly, and data transfers are much faster than the parallel port interfaces common on many FPGA experimentation boards.

On-board Peripherals

The XEM3010 is designed to compactly support a large number of applications with a small number of on-board peripherals. These peripherals are listed below.

Serial EEPROM

A small serial EEPROM is attached to the USB microcontroller on the XEM3010, but not directly available to the FPGA. The EEPROM is used to store boot code for the microcontroller as well as PLL configuration data and a device identifier string.

The PLL configuration data is loaded from EEPROM and used to reconfigure the PLL each time a new configuration file is loaded to the FPGA. Therefore, stable and active clocks will be present on the FPGA pins as soon as it comes out of configuration. The stored PLL configuration may be changed at any time using FrontPanel's PLL Configuration Dialog.

The EEPROM also stores a device identifier string which may be changed at any time using FrontPanel. The string serves only a cosmetic purpose and is used when multiple XEM devices are attached to the same computer so you may select the proper active device.

Cypress CY22393 PLL

A multi-output, triple-PLL clock generator can provide up to five clocks, three to the FPGA and another two to the expansion connectors JP2 and JP3. The PLL is driven by a 48-MHz signal output from the USB microcontroller. The PLL can output clocks up to 150-MHz and is configured through the FrontPanel software interface or the FrontPanel API.

Xilinx Configuration PROM

An 8-Mbit Xilinx PROM (XCF08P) is included on some variants of the XEM3010. This PROM allows the XEM3010 to operate without its USB tether by automatically configuring the on-board FPGA during power-up. This PROM may be programmed over the board's JTAG port using a Xilinx configuration cable and the iMPACT software.

32-MByte Word-Wide Synchronous DRAM

The XEM also includes a 32-MByte SDRAM with a full 16-bit word-wide interface to the FPGA. This SDRAM is attached exclusively to the FPGA and does not share any pins with the expansion connector. The maximum clock rate of the SDRAM is 133 MHz.

The SDRAM is a Micron MT48LC16M16A2BG-75:D (or compatible).

LEDs and Pushbuttons

Eight LEDs and two pushbuttons are available for general use as debug inputs and outputs.

Expansion Connectors

Two high-density, 80-pin expansion connectors are available on the bottom-side of the XEM3010 PCB. These expansion connectors provide user access to several power rails on the XEM3010, two clock generator outputs, four FPGA clock inputs, the USB microcontroller I2C lines, the JTAG chain, and 116 non-shared I/O pins on the FPGA.

The connectors on the XEM3010 are Samtec part number: BSE-040-01-F-D-A. The table below lists the appropriate Samtec mating connectors along with the total mated height.

Samtec Part Number	**Mated Height**
BTE-040-01-F-D-A	5.00mm (0.197")
BTE-040-02-F-D-A	8.00mm (0.315")
BTE-040-03-F-D-A	11.00mm (0.433")
BTE-040-04-F-D-A	16.10mm (0.634")
BTE-040-05-F-D-A	19.10mm (0.752")

FrontPanel Support

The XEM3010 is fully supported by Opal Kelly's FrontPanel software. FrontPanel augments the limited peripheral support with a host of PC-based virtual instruments such as LEDs, hex displays, pushbuttons, toggle buttons, and so on. Essentially, this makes your PC a reconfigurable I/O board and adds enormous value to the XEM3010 as an experimentation or prototyping system.

Programmer's Interface

In addition to complete support within FrontPanel, the XEM3010 is also fully supported by the FrontPanel programmer's interface (API), a powerful C++ class library available to Windows and Linux programmers allowing you to easily interface your own software to the XEM.

In addition to the C++ library, wrappers have been written for Java and Python making the API available under those languages as well. Java and Python extensions are available under Windows and Linux. Sample wrappers are also provided for Matlab and LabVIEW.

Complete documentation and several sample programs are installed with FrontPanel.

Applying the XEM3010

Host Interface

There are 24 pins that connect the on-board USB microcontroller to the FPGA. These pins comprise the host interface on the FPGA and are used for configuration downloads. After configuration, these pins are used to allow FrontPanel communication with the FPGA.

If the FrontPanel okHostInterface module is instantiated in your design, you must map the interface pins to specific pin locations using Xilinx LOC constraints. This may be done using the Xilinx constraints editor or specifying the constraints manually in a text file. An example is shown below:

Xilinx constraints for okHostInterface pin mappings:

```
NET “hi_in<0>”          LOC = “N10”;
NET “hi_in<1>”          LOC = “V2”;
NET “hi_in<2>”          LOC = “V3”;
NET “hi_in<3>”          LOC = “V12”;
NET “hi_in<4>”          LOC = “R8”;
NET “hi_in<5>”          LOC = “T8”;
NET “hi_in<6>”          LOC = “V8”;
NET “hi_in<7>”          LOC = “V7”;
NET “hi_out<0>”         LOC = “V10”;
NET “hi_out<1>”         LOC = “V11”;
NET “hi_inout<0>”       LOC = “T7”;
NET “hi_inout<1>”       LOC = “R7”;
NET “hi_inout<2>”       LOC = “V9”;
NET “hi_inout<3>”       LOC = “U9”;
NET “hi_inout<4>”       LOC = “P11”;
NET “hi_inout<5>”       LOC = “N11”;
NET “hi_inout<6>”       LOC = “R12”;
NET “hi_inout<7>”       LOC = “T12”;
NET “hi_inout<8>”       LOC = “U6”;
NET “hi_inout<9>”       LOC = “V5”;
NET “hi_inout<10>”      LOC = “U5”;
NET “hi_inout<11>”      LOC = “V4”;
NET “hi_inout<12>”      LOC = “U4”;
NET “hi_inout<13>”      LOC = “T4”;
NET “hi_inout<14>”      LOC = “T5”;
NET “hi_inout<15>”      LOC = “R5”;
```

Each of the samples installed with FrontPanel includes a copy of a template constraints file that lists all the XEM3010 pins and maps them to the appropriate FPGA pins using LOC (location) constraints. You can use this template to quickly get the pin locations correct on a new design.

MUXSEL

MUXSEL is a signal on the XEM3010 which selects the signal path to the FPGA programming signals D0 and CCLK. When low (deasserted), the FPGA and USB microcontroller are connected. When high (asserted), the FPGA and PROM are connected.

In normal USB-programmed operation, J1 is inserted pulling MUXSEL low and connecting the FPGA and USB microcontroller at all times. This allows USB-based programming of the FPGA and subsequent USB communication with the FPGA design after configuration.

In order to allow the PROM to configure the FPGA, J1 must be removed. In order to deassert MUXSEL post-configuration, your design must deassert MUXSEL. This allows the FPGA design to properly startup and allows for communication over USB even after the PROM has configured it.

The end result is that your FPGA design should tie HI_MUXSEL to 0. This is the case regardless of how the design was configured (via PROM or USB) and even if you have a PROM-less version of the XEM3010. For example, in Verilog:

```
assign hi_muxsel = 1’b0;
```

I^{2}C Connections

The FPGA on the XEM3010 is attached to the I^{2}C lines from the USB microcontroller. In order to avoid contention with the I^{2}C bus, these lines should be set to high-impedance within your design. If this is not done, FrontPanel may timeout or hang when trying to communicate with the XEM3010, particularly when programming the on-board PLL.

The following lines in your UCF (contraints) file will attach pull-ups to the I^{2}C lines:

```
NET "i2c_scl"      LOC = "U13" | PULLUP;
NET "i2c_sda"      LOC = "R13" | PULLUP;
```

In addition, you will need to set these signals to high-impedance in your HDL. Here is an example of how to do this in Verilog:

```
assign i2c_sda = 1'bz;
assign i2c_scl = 1'bz;
```

LEDs and Pushbuttons

There are eight LEDs and two pushbuttons on the XEM3010. Each is wired directly to the FPGA according to the pin mapping tables at the end of this document.

The LED anodes are connected to a pull-up resistor to +3.3VDD and the cathodes wired directly to the FPGA. To turn ON an LED, the FPGA pin should be brought low. To turn OFF an LED, the FPGA pin should be brought high.

The pushbuttons are connected between their respective FPGA pin and DGND. The FPGA side of the connection has a pull-up resistor to +2.5VDD. Therefore, in the pressed state, the FPGA pin will be at DGND (low) and in the unpressed state, the FPGA pin will be at +2.5VDD (high). Note that the pushbuttons are not debounced on the XEM3010. In order to deglitch the signals from the pushbuttons, proper debouncing should be done inside the FPGA.

Reconfiguration Using S1

When a jumper is installed across J2, S1 is electrically connected to the PROG_B pin on the FPGA. In this configuration, S1 may be used to force the FPGA to reprogram itself using the image in PROM.

Note that this mode is only available when the XEM3010 is configured for PROM configuration of the FPGA. When the XEM3010 is configured for USB configuration, no jumper should be installed across J2.

PLL Connections

The PLL contains six output pins, one of which is left unconnected. The other five are labelled SYS_CLK1 through SYS_CLK5. SYS_CLK4 connects to JP2 and SYS_CLK5 connects to JP3. The other three pins are connected directly to the FPGA. The pin mapping table at the end of this document details the PLL connections.

SDRAM Clock

The SDRAM clock pin (U14-F2) is connected to SYS_CLK1 which is CLKA on the Cypress CY22393 PLL (U8-10). Note that this connection is shared with FPGA GCLK3 (U11-N9).

JTAG

JP1 - JTAG Connector

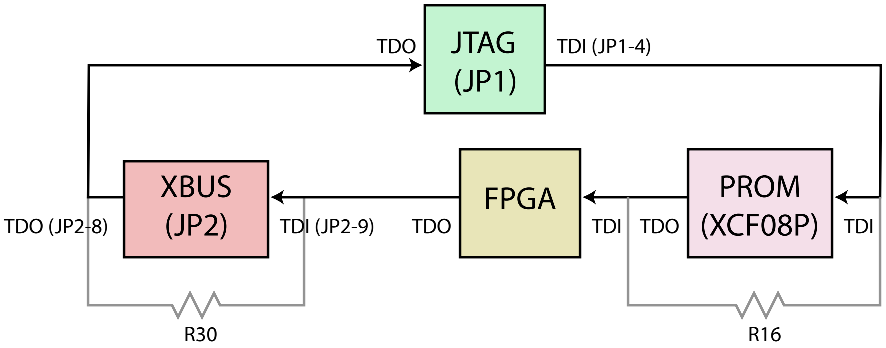
JP1 is the 2mm, 6-pin JTAG connector on-board and connects to the on-board JTAG chain which includes the FPGA, configuration PROM, and expansion connector. These pins can be connected to an external JTAG command converter (such as the Xilinx JTAG cables) for additional programming capability. The JP1 pins are connected as shown below:

JP1 Pin	Signal
1	+2.5VDD
2	TMS
3	TCK
4	TDI
5	DGND
6	TDO

JTAG Connection Chain

The JTAG chain is configured as shown in the diagram below. The PROM and expansion port of this chain may be bypassed using optional 0-Ω resistors, as shown. R16 bypasses the PROM and has been inserted on PROM-less versions of the XEM3010. R16 is not inserted on XEM3010 versions with the PROM.

R30 bypasses the expansion connector and has been inserted on all versions of the XEM3010. If your application places additional components in the JTAG chain, you must remove R30. Note that the JTAG signal level on the XEM3010 is 2.5-v. If your expansion board extends this chain, it must also operate at 2.5-v or use level translation to be compatible.



SDRAM Connections

The Micron SDRAM is connected exclusively to the 3.3v I/O on Bank 0 and Bank 1 of the FPGA. The tables below list these connections.

SDRAM Pin	FPGA Pin
CLK	N9
CKE	F8
$\overline{\text{CS}}$	E8
$\overline{\text{WE}}$	E7
$\overline{\text{CAS}}$	E11
$\overline{\text{RAS}}$	D12
BA0	C12
BA1	A14
LDQM	D9
UDQM	A9
A0	A15
A1	A16
A2	B15
A3	B14
A4	D11
A5	B13
A6	C11
A7	A12
A8	A11
A9	D10

SDRAM Pin	FPGA Pin
A10	A17
A11	B10
A12	A10
D0	C4
D1	D5
D2	C5
D3	D6
D4	D7
D5	C7
D6	C8
D7	D8
D8	B9
D9	A8
D10	A7
D11	B6
D12	A5
D13	B5
D14	A4
D15	B4

Clock Configuration

The XEM3010 has been designed to support SDRAM clocking in both “system synchronous” and “source synchronous” modes. Both configurations are often referenced in Xilinx application notes describing SDRAM controllers and interfaces.

System Synchronous

In this mode, the clock signal is sourced at the system level by the PLL on the XEM3010. The same clock is fanned-out to both the FPGA (pin N9) and the SDRAM (CLK). The FPGA, therefore considers this signal an input and synchronizes its logic fabric to it, typically using a DCM.

Source Synchronous

In this mode, the clock signal is sourced by the FPGA rather than the PLL. To avoid signal contention, the corresponding output (SYS_CLK1) on the PLL must be disabled or increased power consumption and potential damage may be done.

The FPGA pin N9 is configured as an output and provides the clock signal to the SDRAM. Typically, this setup uses the DDR features of the IOB to provide a clock that is well-synchronized with the signals output to and input from the SDRAM, thus minimizing signal skew with respect to the clock.

Expansion Connectors

JP2

JP2 is an 80-pin high-density connector providing access to FPGA Banks 2 and 3. Pins 77 and 79 of this connector are wired to global clock inputs on the FPGA and can therefore be used as inputs to the global clock network.

Pin 11 on this connector is SYSCLK4 and is directly connected to CLKD on the Cypress CY22393 PLL. Using FrontPanel's PLL Configuration Dialog, you can configure the clock signal present on this pin.

Pin mappings for JP2 are listed at the end of this document in the "Quick Reference" section. For each JP2 pin, the corresponding board connection is listed. For pins connected to the FPGA, the corresponding FPGA pin number is also shown. Finally, for pins routed to differential pair I/Os on the FPGA, the FPGA signal names and routed track lengths have been provided to help you equalize lengths on differential pairs.

JP3

JP3 is an 80-pin high-density connector providing access to FPGA Banks 6 and 7. Pins 77 and 79 of this connector are wired to global clock inputs on the FPGA and can therefore be used as inputs to the global clock network.

Pin 8 on this connector is SYSCLK5 and is directly connected to CLKE on the Cypress CY22393 PLL. Using FrontPanel's PLL Configuration Dialog, you can configure the clock signal present on this pin.

Pin mappings for JP3 are listed at the end of this document in the "Quick Reference" section. For each JP3 pin, the corresponding board connection is listed. For pins connected to the FPGA, the corresponding FPGA pin number is also shown. Finally, for pins routed to differential pair I/Os on the FPGA, the FPGA signal names and routed track lengths have been provided to help you equalize lengths on differential pairs.

Setting I/O Voltages

The Spartan-3 FPGA allows users to set I/O bank voltages in order to support several different I/O signalling standards. This functionality is supported by the XEM3010 by allowing the user to connect independent supplies to the FPGA VCCO pins on four of the FPGA banks.

By default, ferrite beads have been installed which attach each VCCO bank to the +3.3VDD supply. If you intend to supply power to a particular I/O bank, you MUST remove the appropriate ferrite beads. Power can then be supplied through the expansion connectors.

The table below lists details for user-supplied I/O bank voltages

I/O Bank	Expansion Pin	FPGA Pins	Ferrite Bead
2	JP2-55	J12, H12, F16	FB2
3	JP2-35	N16, L12, K12	FB3
6	JP3-36	K7, L7, N3	FB4
7	JP3-56	F3, H7, J7	FB5

Clock Inputs and Bank Voltages

Note that the four clock inputs available on the expansion connectors are connected to FPGA banks 0 and 1. Bank voltages for these two banks are fixed on the XEM3010 to +3.3VDD. However, Xilinx Answer Record #18095 states:

> Differential Input Buffers are powered by VCCAUX and are not VCCO-dependent. Consequently, you can put LVDS_25 and LVPECL_25 input buffers in a 3.3V bank without damaging the device. Instantiating a LVDS_25 or LVPECL_25 input buffer in 3.3V bank does not generate a software error.

For more information on this, please refer to the Xilinx Answer Record and other references available within that record.

Power-On I/O State (PCB revision 20070117)

In all versions of the XEM3010 PCB prior to 20070117 (YYYYMMDD datecode), the HSWAP_EN pin (E6 on the FPGA) was directly connected to DGND. This enables pull-up resistors on all User I/Os from power-on throughout configuration. (See the Spartan-3 Data Sheet from Xilinx).

With version 20070117, a 0-Ω resistor has been added (R43). By default, this resistor IS NOT LOADED. This resistor connects HSWAP_EN to DGND. Therefore, for version 20070117 there are two possible configurations:

Remove R43 (Default Configuration)

HSWAP_EN is allowed to float and an internal pull-up pulls HSWAP_EN high. This disables the user I/O pull-up resistors allowing the I/Os to float from power-on throughout configuration.

Insert R43 (0-Ω Resistor)

HSWAP_EN is grounded. This enables user I/O pull-up resistors from power-on throughout configuration. See the Xilinx Spartan-3 Data Sheet for details regarding the characteristics of these pull-ups.

Considerations for Differential Signals

The XEM3010 PCB layout and routing has been designed with several applications in mind, including applications requiring the use of differential (LVDS) pairs. Please refer to the Xilinx Spartan-3 datasheet for details on using differential I/O standards with the Spartan-3 FPGA.

FPGA I/O Bank Voltages

In order to use differential I/O standards with the Spartan-3, you must set the VCCO voltages for the appropriate banks to 2.5v according to the Xilinx Spartan-3 datasheet. Please see the section above entitled "Setting I/O Voltages" for details.

Characteristic Impedance

The characteristic impedance of all routes from the FPGA to the expansion connector is 50-Ω, with the exception of routes that are labelled with (†) in the mapping table. These exception routes are routed on inner layers without a proximity ground plane and therefore do not match the 50-Ω impedance exactly.

Differential Pair Lengths

In many cases, it is desirable that the route lengths of a differential pair be matched within some specification. Care has been taken to route differential pairs on the FPGA to adjacent pins on the expansion connectors whenever possible. We have also included the lengths of the board routes for these connections to help you equalize lengths in your final application. Due to space constraints, some pairs are better matched than others.

Digitally Controlled Impedance (DCI)

The Xilinx Spartan-3 supports digitally controlled impedance. This functionality is supported when precision resistors are connected externally between the FPGA VRN/VRP lines and +VCCO/DGND, respectively. Pads for these resistors have been placed and routed on the XEM3010, but resistors have NOT been installed. The end-user must install these resistors in order to use DCI. The table below lists the resistor designators and the banks they control.

Resistor	FPGA Pin	FPGA Signal	Connection
R22	C17	L01P_2/VRN_2	+VCCO2
R24	C16	L01N_2/VRP_2	DGND
R21	T16	L01P_3/VRN_3	+VCCO3
R23	T17	L01N_3/VRP_3	DGND
R18	T2	L01P_6/VRN_6	+VCCO6
R20	T3	L01N_6/VRP_6	DGND
R17	C2	L01P_7/VRN_7	+VCCO7
R19	C3	L01N_7/VRP_7	DGND

BRK3010 Breakout Board

The BRK3010 is a simple two-layer "breakout board" which can be used to evaluate or transition to the XEM3010. It provides standard 0.1" thru-hole connections to the 0.8-mm high-density connectors on the XEM3010.

The corresponding connections to the XEM3010 are labelled in silkscreen on the BRK3010. The BRK3010 connectors essentially mirror the connections on the XEM3010, left to right. For example, the JP2 connector on the XEM3010 is electrically connected to JP1/JP2 on the BRK3010 according to the table below. A similar mapping exists for JP3 on the XEM3010.

BRK3010	XEM3010
JP1-1	JP2-2
JP1-2	JP2-1
JP1-3	JP2-4
JP1-4	JP2-3
...	...
JP2-38	JP2-77
JP2-39	JP2-80
JP2-40	JP2-79

Xilinx Configuration PROM

Some versions of the XEM3010 are built with a Xilinx configuration PROM inserted. This PROM allows the FPGA to be configured upon power-up without a USB connection as some applications may require the FPGA to control a user's device and only occasionally be connected to a PC. The USB connection may therefore be used for extracting acquired data, adjusting parameters, and so on.

Getting the XEM3010 to boot from a PROM-based FPGA configuration is a multistep process consisting of the following steps:

1. Generate an FPGA programming file.
2. Generate a PROM programming file from the FPGA programming file.
3. Program the PROM.

Generate an FPGA Programming File.

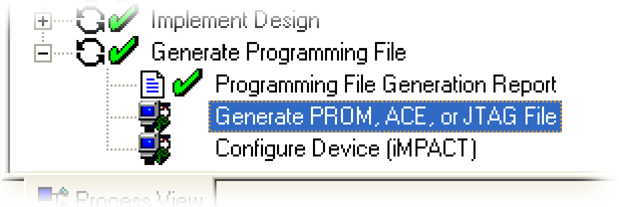
This step is performed for either PROM-boot or USB-boot and is the final step in a typical FPGA synthesis flow. It is assumed that the user is already familiar with this procedure and it will not be covered here.

Generate a PROM Programming File

In this step, the Xilinx iMPACT tool is used to format a PROM programming file with the FPGA programming file created previously. In the next step, the PROM programming file will be transferred (e.g. via JTAG) to the PROM.

Start iMPACT

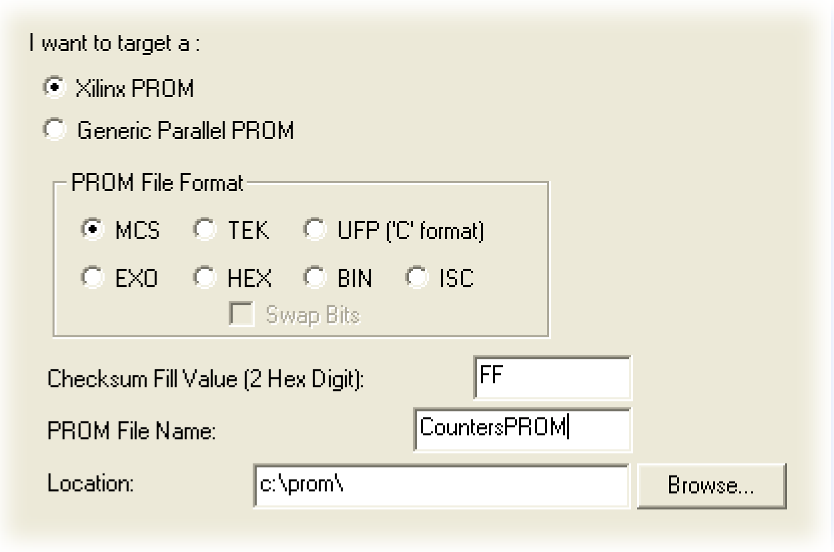
Once the FPGA programming file (bitfile) has been created, you can start iMPACT from within Project Navigator by clicking on "Generate PROM, ACE, or JTAG File" in the processes list.



This will start iMPACT. When asked, tell it you would like to create a PROM File.

Setup PROM File Format

At the next screen, select "Xilinx PROM" as a target with the "MCS" format. Here you can also specify a filename for your programming file.



I want to target a :

● Xilinx PROM

○ Generic Parallel PROM

PROM File Format

● MCS ○ TEK ○ UFP ('C' format)

○ EXO ○ HEX ○ BIN ○ ISC

☐ Swap Bits

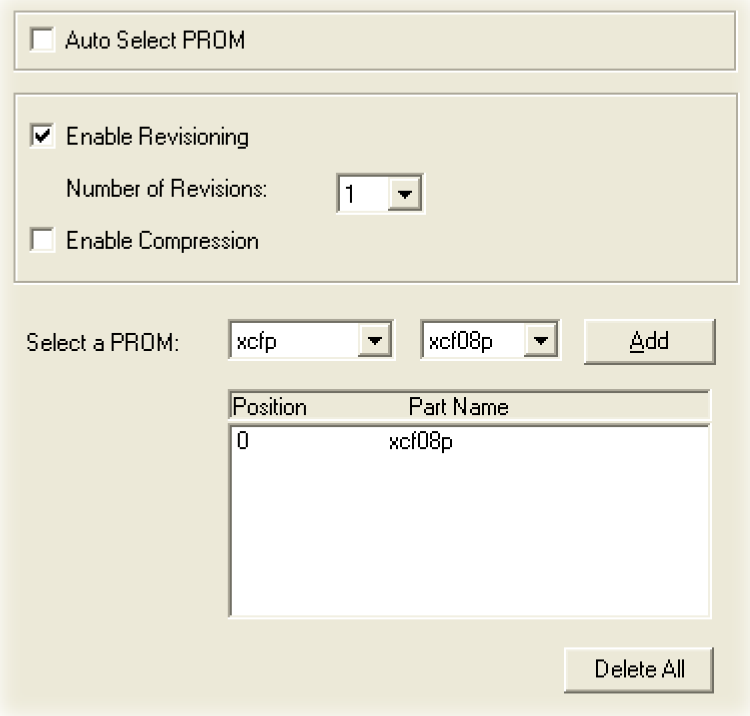
Checksum Fill Value (2 Hex Digit): FF

PROM File Name: CountersPROM

Location: c:\prom\

Select the PROM Device

At the next screen, check "Enable Revisioning". This is necessary in order to enable some features of the Xilinx PROM that allow it to boot the FPGA as a programming master. Select the PROM device as "xcf08p," the device on the XEM3010, and add it to the list.



☐ Auto Select PROM

☑ Enable Revisioning

Number of Revisions: 1

☐ Enable Compression

Select a PROM: xcfp xcf08p

Position	Part Name
0	xcf08p

Add Bitfiles to PROM

The final step in creating the PROM is to add your bitfile to the PROM. Simply select the file (e.g. counters.bit) that you generated previously. Once you complete the Wizard, the MCS programming file will be created in the directory specified. In our case, we have CountersPROM.mcs.

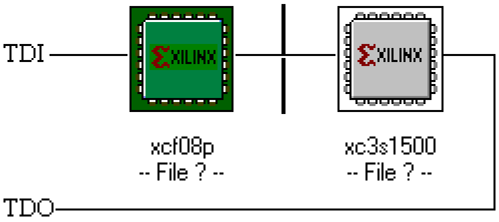
Programming the Configuration PROM

Once we have a PROM programming file, we can transfer that file to the Xilinx Configuration PROM on the XEM3010 using a JTAG cable. The Xilinx Parallel IV or Xilinx USB JTAG cables will work just fine for this process.

Connecting to the JTAG Chain

At this point, you may attach your programming cable to the XEM3010. Be sure to connect the pins correctly or you could damage the XEM3010 or the programming cable.

If you are still in iMPACT, you can switch to Configuration Mode using the “Mode” menu at the top of the window. Allow iMPACT to automatically discover the JTAG chain and you will end up with a graphical representation of the chain.



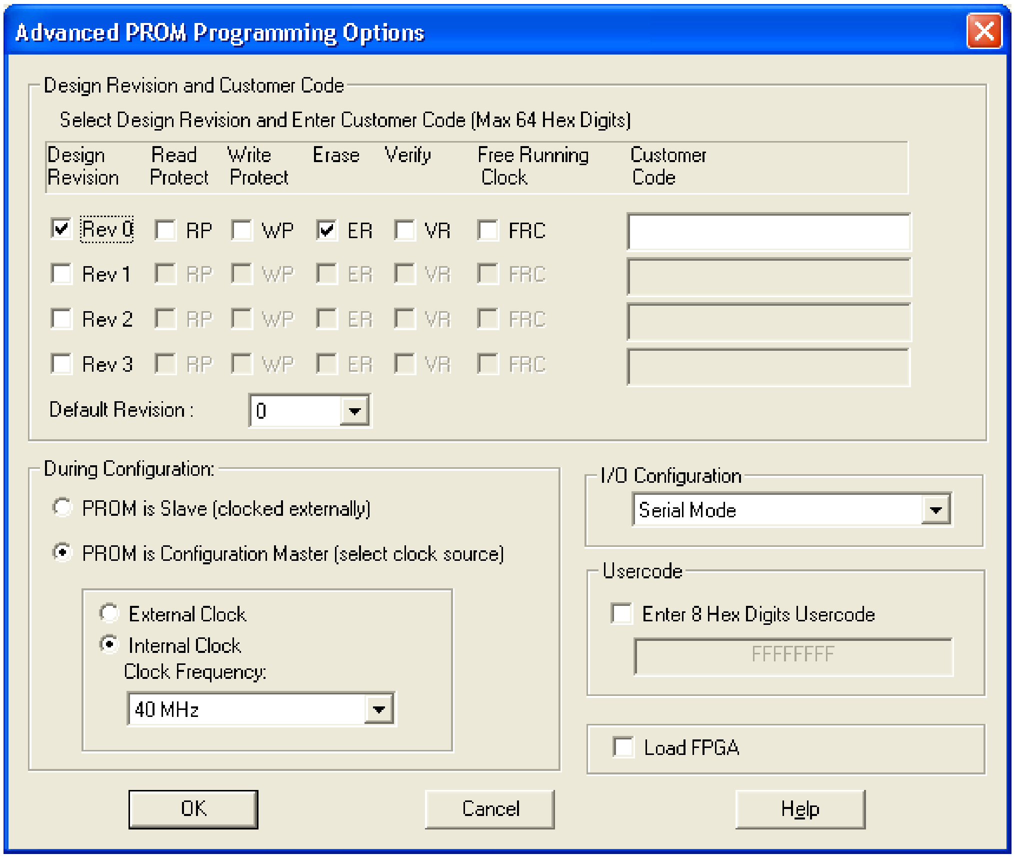
Assign the PROM Configuration File

Assign the PROM configuration file (CountersPROM.mcs) that you created in the previous step to the XCF08P device. You may bypass the XC3S1500 device since we will only be configuring the PROM.

Program the PROM

Once a configuration file has been assigned to the PROM device, you will be able to program it by right-clicking on the device and selecting “Program...” from the context menu. In the options dialog, setup the following options:

- Select Rev 0 and “ER” to erase any existing configuration
- PROM is Configuration Master
- Internal Clock
- Clock Frequency set to 40 MHz
- I/O Configuration is Serial Mode



Advanced PROM Programming Options

Design Revision and Customer Code

Select Design Revision and Enter Customer Code (Max 64 Hex Digits)

Design Revision	Read Protect	Write Protect	Erase	Verify	Free Running Clock	Customer Code
☑ Rev 0	☐ RP	☐ WP	☑ ER	☐ VR	☐ FRC	
☐ Rev 1	☐ RP	☐ WP	☐ ER	☐ VR	☐ FRC	
☐ Rev 2	☐ RP	☐ WP	☐ ER	☐ VR	☐ FRC	
☐ Rev 3	☐ RP	☐ WP	☐ ER	☐ VR	☐ FRC	

Default Revision : 0

During Configuration:

○ PROM is Slave (clocked externally)

● PROM is Configuration Master (select clock source)

○ External Clock

● Internal Clock

Clock Frequency: 40 MHz

I/O Configuration: Serial Mode

Usercode

☐ Enter 8 Hex Digits Usercode

FFFFFFFF

☐ Load FPGA

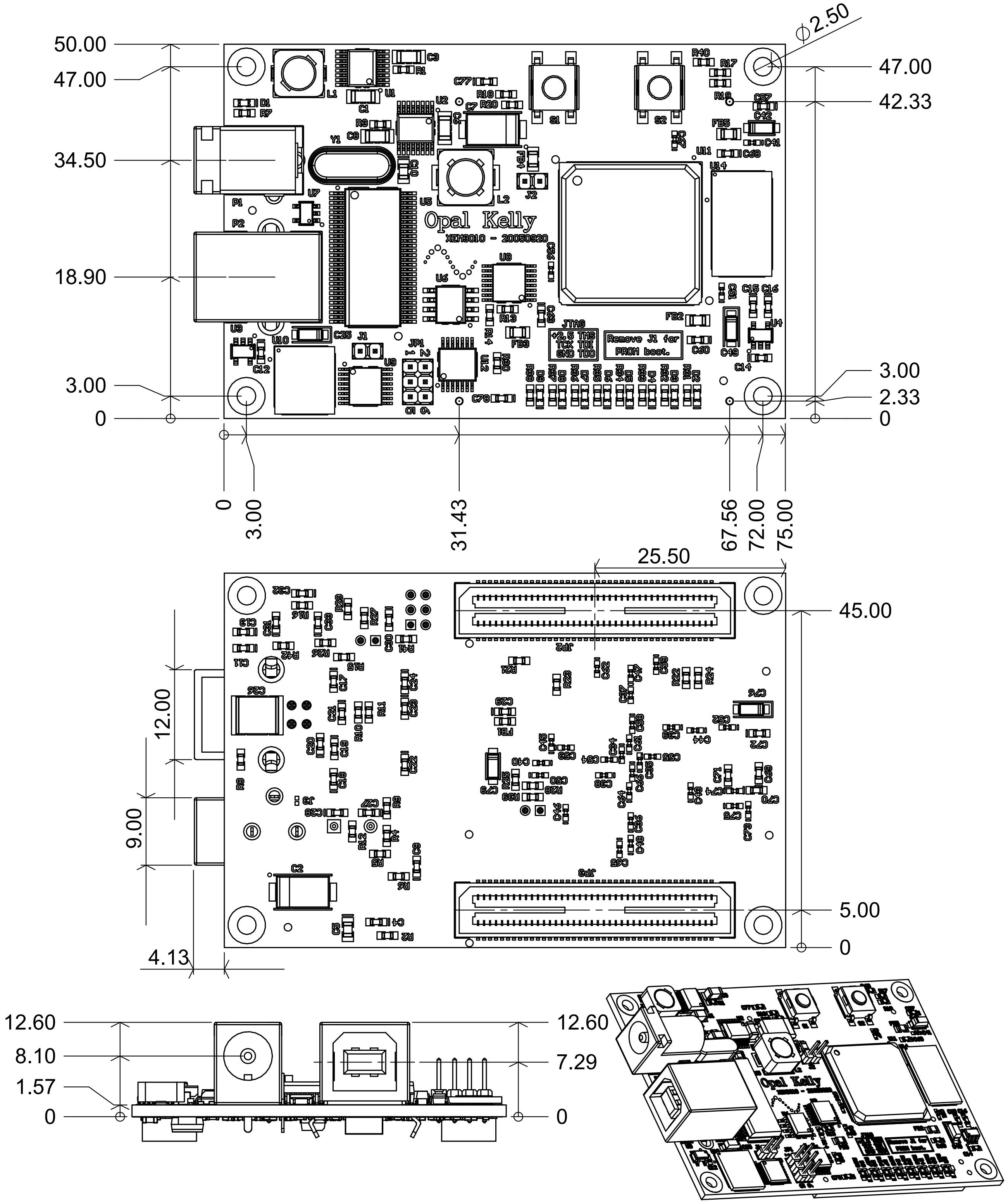
Once you acknowledge this dialog, the programming operation will start. Once complete, the PROM should be setup with your new FPGA programming file!

Booting from PROM

In order to boot the XEM3010 from PROM, you must remove the jumper on J1. This allows the PROM to configure the FPGA from power-on.

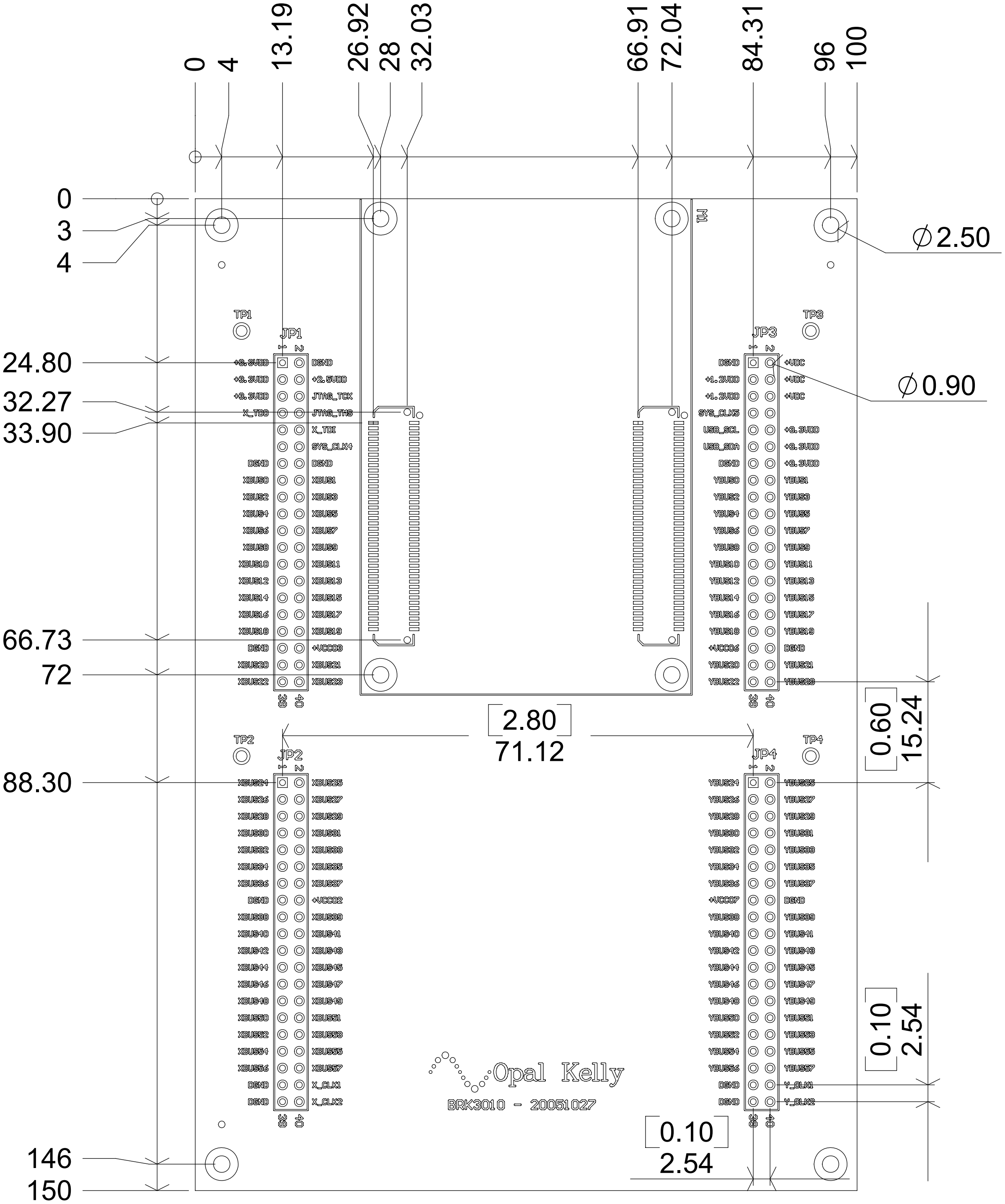
If your FPGA design has MUXSEL=0, the design will still be able to communicate with FrontPanel if it is connected to a PC.

XEM3010 Mechanical Drawing



All dimensions in mm.

BRK3010 Mechanical Drawing



All dimensions in mm.
[inches]

XEM3010 Quick Reference

JP2 Pin	Connection	FPGA Pin	LVDS	Length (mm)
1	DGND			
3	+2.5VDD			
5	JTAG_TCK			
7	JTAG_TMS			
9	X_TDI			
11	SYS_CLK4			
13	DGND			
15	XBUS-1	T16 (*)	L01P_3	17.196
17	XBUS-3	T17 (*)	L01N_3	12.588
19	XBUS-5	R16	L17P_3	13.817
21	XBUS-7	P15	L21N_3	14.607
23	XBUS-9	P16	L17N_3	13.276
25	XBUS-11	N15	L21P_3	14.359
27	XBUS-13	M15	L23N_3	14.442
29	XBUS-15	M16	L23P_3	13.110
31	XBUS-17	L15	L34N_3	16.068
33	XBUS-19	L16	L34P_3	14.736
35	+VCCO3			
37	XBUS-21	N14 (†)	L22P_3	13.950
39	XBUS-23	M14 (†)	L22N_3	14.282
41	XBUS-25	K13 (†)	L39N_3	14.951
43	XBUS-27	K14 (†)	L39P_3	13.619
45	XBUS-29	K15	-	12.288
47	XBUS-31	J14 (†)	L40P_2	14.316
49	XBUS-33	J15	L40N_2	12.868
51	XBUS-35	G14 (†)	L22P_2	16.068
53	XBUS-37	F14 (†)	L22N_2	15.736
55	+VCCO2			
57	XBUS-39	H16	L34N_2	10.791
59	XBUS-41	H15	L34P_2	12.163
61	XBUS-43	G16	L24P_2	11.205
63	XBUS-45	G15	L24N_2	12.205
65	XBUS-47	F15	L21N_2	12.039
67	XBUS-49	E16	L19P_2	10.956
69	XBUS-51	E15	L21P_2	12.288
71	XBUS-53	D16	L19N_2	11.205
73	XBUS-55	C17 (*)	L01P_2	10.785
75	XBUS-57	C16 (*)	L01N_2	11.453
77	XCLK1	F10	L32P_1	21.992
79	XCLK2	E10	L32N_1	21.756

JP2 Pin	Connection	FPGA Pin	LVDS	Length (mm)
2	+3.3VDD			
4	+3.3VDD			
6	+3.3VDD			
8	X_TDO			
10	-			
12	-			
14	DGND			
16	XBUS-0	U18	L16P_3	17.089
18	XBUS-2	T18	L16N_3	17.172
20	XBUS-4	R17	L19N_3	18.255
22	XBUS-6	R18	L19P_3	16.923
24	XBUS-8	P17	L20P_3	18.006
26	XBUS-10	P18	L20N_3	16.675
28	XBUS-12	N17	L24P_3	17.757
30	XBUS-14	M18	L24N_3	17.426
32	XBUS-16	L17	L35P_3	18.450
34	XBUS-18	L18	L35N_3	16.885
36	DGND			
38	XBUS-20	K17	L40N_3	17.509
40	XBUS-22	K18	L40P_3	16.509
42	XBUS-24	L14 (†)	L27N_3	19.266
44	XBUS-26	L13 (†)	L27P_3	19.935
46	XBUS-28	J13 (†)	-	21.426
48	XBUS-30	H13 (†)	L27N_2	22.119
50	XBUS-32	H14 (†)	L27P_2	20.539
52	XBUS-34	J18	L39N_2	15.680
54	XBUS-36	J17	L39P_2	16.929
56	DGND			
58	XBUS-38	H18	L35P_2	15.515
60	XBUS-40	H17	L35N_2	16.680
62	XBUS-42	G18	L23N_2	15.515
64	XBUS-44	F17	L23P_2	15.686
66	XBUS-46	E18	L20P_2	14.355
68	XBUS-48	E17	L20N_2	15.686
70	XBUS-50	D18	L17P_2	15.018
72	XBUS-52	D17	L17N_2	16.101
74	XBUS-54	C18	L16P_2	14.852
76	XBUS-56	B18	L16N_2	16.601
78	DGND			
80	DGND			

Notes: * - Pin is a DCI pin with optionally-installed resistors.
† - Some routing on inner layer is not necessarily 50Ω.

Host Interface Pin	FPGA Pin
HI_IN[0]	N10
HI_IN[1]	V2
HI_IN[2]	V3
HI_IN[3]	V12
HI_IN[4]	R8
HI_IN[5]	T8
HI_IN[6]	V8
HI_IN[7]	V7
HI_OUT[0]	V10
HI_OUT[1]	V11
HI_INOUT[0]	T7
HI_INOUT[1]	R7
HI_INOUT[2]	V9
HI_INOUT[3]	U9
HI_INOUT[4]	P11
HI_INOUT[5]	N11
HI_INOUT[6]	R12
HI_INOUT[7]	T12
HI_INOUT[8]	U6
HI_INOUT[9]	V5
HI_INOUT[10]	U5
HI_INOUT[11]	V4
HI_INOUT[12]	U4
HI_INOUT[13]	T4
HI_INOUT[14]	T5
HI_INOUT[15]	R5

LED	FPGA Pin
D2	V14
D3	U14
D4	T14
D5	V15
D6	U15
D7	V16
D8	V17
D9	U16

Button	FPGA Pin
S1	P7
S2	P6

PLL Pin	Clock Name	Connection
CLKA	SYS_CLK1	FPGA - N9
CLKB	SYS_CLK2	FPGA - P9
CLKC	SYS_CLK3	FPGA - P10
CLKD	SYS_CLK4	JP2-11
CLKE	SYS_CLK5	JP3-8
XBUF	N/A	Not Connected

XEM3010 Quick Reference

JP3 Pin	Connection	FPGA Pin	LVDS	Length (mm)
1	+VDC			
3	+VDC			
5	+VDC			
7	-			
9	+3.3VDD			
11	+3.3VDD			
13	+3.3VDD			
15	YBUS-1	U1	L16N_6	17.689
17	YBUS-3	T1	L16P_6	17.772
19	YBUS-5	R2	L17N_6	18.855
21	YBUS-7	R1	L17P_6	17.523
23	YBUS-9	P2	L20N_6	18.606
25	YBUS-11	P1	L20P_6	17.275
27	YBUS-13	N2	L24N_6	18.357
29	YBUS-15	M1	L24P_6	17.967
31	YBUS-17	L2	L35N_6	19.050
33	YBUS-19	L1	L35P_6	17.719
35	DGND			
37	YBUS-21	K2	L40P_6	18.470
39	YBUS-23	K1	L40N_6	17.139
41	YBUS-25	K5 (†)	L39N_6	20.280
43	YBUS-27	K4 (†)	L39P_6	19.612
45	YBUS-29	J6 (†)		22.436
47	YBUS-31	J5 (†)	L40N_7	20.529
49	YBUS-33	J4 (†)	L40P_7	19.198
51	YBUS-35	J1	L39N_7	17.602
53	YBUS-37	J2	L39P_7	18.485
55	DGND			
57	YBUS-39	H1	L35N_7	16.446
59	YBUS-41	H2	L35P_7	17.446
61	YBUS-43	G1	L23N_7	16.032
63	YBUS-45	F2	L23P_7	16.618
65	YBUS-47	E1	L20P_7	16.612
67	YBUS-49	E2	L20N_7	17.612
69	YBUS-51	D1	L17N_7	16.198
71	YBUS-53	D2	L17P_7	17.198
73	YBUS-55	C1	L16N_7	15.784
75	YBUS-57	B1	L16P_7	15.369
77	YCLK1	E9	L32N_0	29.060
79	YCLK2	F9	L32P_0	30.743

JP3 Pin	Connection	FPGA Pin	LVDS	Length (mm)
2	DGND			
4	+1.2VDD			
6	+1.2VDD			
8	SYS_CLK5			
10	USB_SCL			
12	USB_SDA			
14	DGND			
16	YBUS-0	T3 (*)	L01N_6	15.573
18	YBUS-2	T2 (*)	L01P_6	17.182
20	YBUS-4	R3	L19N_6	14.125
22	YBUS-6	P4	L21P_6	15.207
24	YBUS-8	P3	L19P_6	13.876
26	YBUS-10	N4	L21N_6	14.959
28	YBUS-12	M4	L23P_6	15.042
30	YBUS-14	M3	L23N_6	13.876
32	YBUS-16	L4	L34P_6	15.320
34	YBUS-18	L3	L34N_6	14.155
36	+VCCO6			
38	YBUS-20	N5 (†)	L22N_6	14.302
40	YBUS-22	M5 (†)	L22P_6	14.053
42	YBUS-24	L5 (†)	L27P_6	14.136
44	YBUS-26	L6 (†)	L27N_6	14.805
46	YBUS-28	K6	-	16.423
48	YBUS-30	H6 (†)	L27P_7	16.213
50	YBUS-32	H5 (†)	L27N_7	14.882
52	YBUS-34	G5 (†)	L22N_7	15.185
54	YBUS-36	F5 (†)	L22P_7	15.048
56	+VCCO7			
58	YBUS-38	H3	L34P_7	11.971
60	YBUS-40	H4	L34N_7	12.971
62	YBUS-42	G3	L24P_7	11.556
64	YBUS-44	G4	L24N_7	12.722
66	YBUS-46	F4	L21P_7	12.971
68	YBUS-48	E3	L19N_7	11.556
70	YBUS-50	E4	L21N_7	13.219
72	YBUS-52	D3	L19P_7	11.805
74	YBUS-54	C2 (*)	L01P_7	16.590
76	YBUS-56	C3 (*)	L01N_7	16.200
78	DGND			
80	DGND			

Notes: * - Pin is a DCI pin with optionally-installed resistors.
† - Some routing on inner layer is not necessarily 50Ω.