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Cryogenic Amplifiers for Interfacing Superconductive Systems to Room Temperature Electronics

by

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Declaration

By submitting this thesis electronically, I declare that the entirety of the work is my own, original work, that I am the owner of the copyright thereof (unless to the extent explicitly otherwise stated) and that I have not previously in its entirety or in part submitted it for obtaining any qualification.

Abstract

This thesis is aimed at testing commercially available CMOS amplifier ICs at 4 K. Super Conducting Electronics (SCE) will also be used to amplify RSFQ signals for easier detection by CMOS technology and better signal-to-noise ratios.

The SCE comprises of a Suzuki stack amplifier, a 250 μA JTL and a DC-to-SFQ converter. The Suzuki stack amplifier is simulated in WRSPICE. It is able to amplify an SFQ signal synchronised with an external clock signal. The amplified signal can then be detected by a normal commercially available CMOS amplifier IC.

To keep the noise in the signal to a minimum, the commercial amplifier must be be situated as close as possible to the SCE. The amplifier must therefore be able to operate at 4 K. Ten different amplifier ICs were tested and three was found that worked down to 4 K.

Opsomming

Hierdie tesis is gemik op die toets van komersieel beskikbare CMOS versterker geïntegreerde stroombane by 4 K. Supergeleier elektronika (SGE) gaan ook gebruik word om RSFQ seine te versterk, sodat dit makliker deur CMOS tegnologie bespeur kan word en 'n beter sein-tot-ruis verhouding kan hê.

Die SGE bestaan uit 'n Suzuki stapel versterker, 'n 250 μA JTL en 'n DC-na-SFQ omskakelaar. Die Suzuki stapel versterker was slegs gesimuleer in WRSPICE. Dit kan 'n SFQ sein versterk en dit sinchroniseer met 'n eksterne klok sein. Die versterkte sein kan dan makliker deur normale komersieël beskikbare CMOS versterkers bespeur word.

Om die ruis van die sein minimaal te hou, moet die komersiële versterkers so na as moontlik aan die SGE wees. Daarom moet die versterker by 4 K kan werk. Tien verskillende versterkers was getoets, waarvan drie kon werk tot by 4 K.

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Nomenclature

Abbreviations

AC	= Alternating Current
BCLDD	= Buried Channel Lightly Doped Drain
CES	= Central Electronic Services
CMOS	= Complementary Metal-Oxide-Semiconductor
COSL	= Complementary Output Switching Logic
DC	= Direct Current
DUT	= Device Under Test
EMI	= ElectroMagnetic Interference
FET	= Field Effect Transistor
HBT	= Heterojunction Bipolar Transistor
HCC-JJ	= Higher Critical Current - Josephson Junction
HEMT	= High Electron Mobility Transistor
I_c	= Critical Current
IC	= Integrated Circuit
JJ	= Josephson Junction
JTL	= Josephson Transmission Line
LCC-JJ	= Lower Critical Current - Josephson Junction
LDD	= Lightly Doped Drain
LNA	= Low Noise Amplifier
LSI	= Large Scale Integration
MMIC	= Monolithic Microwave Integrated Circuit
MOS	= Metal-Oxide-Semiconductor
NMOS	= N-type Metal-Oxide-Semiconductor
PCB	= Printed Circuit Board

p-HEMT = Pseudomorphic - High Electron Mobility Transistor
PMOS = P-type Metal-Oxide-Semiconductor
RF = Radio Frequency
RSFQ = Rapid Single Flux Quantum
SCE = SuperConductive Electronics
SFQ = Single Flux Quantum
SQUID = Superconducting Quantum Interference Device
SMA = Sub-Miniature version A
SMD = Surface Mount Device
SOIC = Small-Outline Integrated Circuit
SPICE = Simulation Program with Integrated Circuit Emphasis
T_c = Critical Temperature

Prefixes

p = pico = 10^{-12}
n = nano = 10^{-9}
μ = micro = 10^{-6}
m = milli = 10^{-3}
k = kilo = 10^{3}
M = mega = 10^{6}
G = giga = 10^{9}

Units

A = Ampere
°C = Degrees Celsius
eV = Electron-Volts ($160.217\ 733\ 0 \cdot 10^{-21}$ J)
Hz = Hertz
K = Kelvin
m = Meters
V = Volt
W = Watt
Ω = Ohm

Chapter 1

Introduction

1.1 Background

The field of applied superconductivity is young and exciting, with new applications appearing regularly. Superconductivity is the phenomenon that occurs in certain materials at extremely low temperatures. It is characterised by exactly zero electrical resistance and the exclusion of the interior magnetic field. At temperatures below the critical temperature (T_c), the resistance disappears almost instantaneously. Each substance has its own critical current ranging from 4.2 K (Mercury) up to 200 K ($Sn_6Ba_4Ca_2Cu_{10}O_y$) [4]. Superconducting electronics (SCE) outperform semiconductors in almost every aspect, but require cryogenic cooling (which requires high vacuum environments) and good magnetic shielding to operate.

Superconductors are used to build Josephson Junctions (JJ), the active device in SCE [5]. It is a junction between two superconductors which is small enough to allow only a slight overlap of the electron pair wave function of the two superconductors. A non-stationary Josephson effect occurs if a constant voltage U or a current larger than the so-called critical current (I_c) is applied to the junction. The junction then acquires an active resistance. As noted by [5] and explained further in section 2.1 on page 4 to be contrary to Ohm's law,

$$I = \frac{U}{R}, \tag{1.1}$$

the voltage U is not proportional to the size of the current, but its frequency,

$$f_J = U\frac{2e}{h}. \tag{1.2}$$

When you substitute the constants, e and h, into equation 1.2, you find that f_J increases by 483.6 MHz / μV. For voltages in the order of milli-volts, the frequencies range from hundreds to thousands of gigahertz. The JJ of two superconductors not only converts a direct voltage into an alternating current, but also functions as an oscillatory circuit.

Josephson junctions form the building blocks of Superconducting Quantum Interference Devices (SQUIDs) and of Rapid Single Flux Quantum RSFQ. A SQUID is the most sensitive magnetometers known at present [5]. RSFQ is a digital electronics technology that relies on quantum effects in superconducting materials to switch signals. Cryogenic cooling requirements have long hindered the entry of superconducting electronics into commercial markets and industrial applications. However, recent advances in cryocooler technology have brought performance and price into the bracket where industrial applications with superconducting electronics can compete with Complementary Metal-Oxide-Semiconductor (CMOS) systems.

The only remaining obstacle to the large scale integration of superconducting electronics into industrial equipment is the interface from cryogenic environments to room temperature electronics. RSFQ output signals are single quanta pulses at the lowest energy level, which make them incompatible with most CMOS electronic devices. The ability to deploy 100 GHz mixed-signal systems or higher will usher in a telecommunications and computer revolution. Specific areas to benefit include the wireless communication industry, the defence market and the hyper-computer business.

1.2 Research Objectives

This thesis is aimed at testing commercially available CMOS amplifier circuitry at 4 Kelvin, or -269 °C. It would plot the S-parameters of different amplifiers at 4 Kelvin. These parameters can then be used to design, verify and construct interface electronics that can successfully operate at 4 K. These electronics can form the basis of most SCE systems, as it would allow out-of-lab usage of SCE systems in industrial environments.

1.3 Thesis Overview

Theoretical studies done showed that the problem can be solved in two parts. First the RSFQ signal can be amplified with the use of superconducting technology. Next the amplified signal can be further amplified with a CMOS amplifier that operate at 4.2 K. The superconducting amplifier was designed and will only be demonstrated with simulations and Monte Carlo analysis. A prototype was not developed due to cost and time restrains.

The cryocooler was modified to accommodate RF input and output signals through two SMA feed-through connectors. Various different commercially available amplifier Integrated Circuits (IC's) were tested inside the cryocooler. The tests were performed with the DUT (device under test) at 4 K and the cryo-cooler in full operation. The results were compared with the room temperature equivalent results. Various different CMOS manufacturing processes were tested and compared with each other. Pseudomorphic-High Electron Mobility Transistors (p-HEMT) were also tested and compared. Practical and simulation results are provided along with conclusions and recommendations.

Chapter 2

Background and Specifications

Superconductive RSFQ electronics are capable of outperforming conventional semiconductor electronics in terms of speed. Superconductive circuits are always accommodated in a cooling system, therefore it is reasonable to cool down the amplifier as well to cryogenic temperatures for the sake of noise reduction and gain improvement. The interfacing of cryogenic electronics with room temperature electronics is a challenging field for amplifier design.

2.1 Josephson Junctions

Josephson junctions are explained by [5]. Two superconductors are placed on top of each other with a non-superconducting barrier placed between them. If the barrier is sufficiently thin (a few nano meters) electrons can pass from one superconductor to the other, although a non-conducting layer exist between the two layers. That is thanks to the quantum mechanical tunneling effect. The wave function, describing the probability of finding an electron, leaks out from the metallic region. If a second metal is brought into this zone, a current can flow across this sandwich structure.

Due to the tunneling electrons, the two superconductors are coupled to each other and a weak supercurrent (Josephson current) can flow across the barrier. A superconductor can carry only a limited constant electric current called the critical current (I_c). Divided by the contact area, we have the critical current density J_c. When an applied current exceeds the J_c of the Josephson

Junction, it returns to its resistive state.

If a direct voltage U is applied to the sandwich, the gauge-invariant phase difference increases as a function of time. That gives a high-frequency alternating current, the frequency of which is given by,

$$f_J = U\frac{2e}{h}. \tag{2.1}$$

Fundamental constants h and e allows us to define the ratio of the junction frequency (f_J) and the applied voltage as 483.6 MHZ / μV.

2.2 SQUID Devices

For SQUID operation, two phenomena are of importance. These are the stationary Josephson effect and the conservation and quantisation of a magnetic flux in a superconducting ring. A SQUID consist of a superconducting ring with one (RF-SQUID) or two (DC-SQUID) Josephson Junctions in parallel.

Figure 2.1 shows the circuit layout of a DC-SQUID. The ring is located in a magnetic field oriented perpendicular to the area of the ring. A bias current (I) flows along the ring. By measuring the voltage drop across the Josephson junction, we can determine the maximum current that can be carried by the ring. This maximum current oscillates as a function of the applied magnetic field or the flux through the ring [5]. An outlet and inlet provides access to the SQUID for current biasing. A DC-SQUID is much more sensitive and stable than a RF-SQUID.

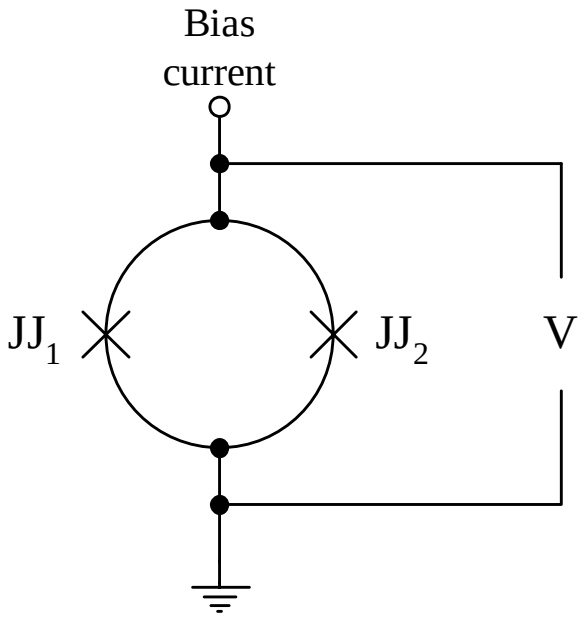


Figure 2.1: Circuit layout of a DC-SQUID.

2.3 RSFQ Signals

As mentioned in Chapter 1, SCE technology holds great potential for the future. RSFQ is a digital electronics technology that relies on quantum effects in superconducting materials to switch signals. A slightly overcritical current is applied to an over damped junction. The Josephson alternating currents flow across the junction in the form of a short pulse (SFQ pulse). According to [5] the width of the pulse is ϕ_0/I_cR. In their example $I_cR = 1$ mV. That gave a pulse width of about 2 ps. During a pulse, the phase difference γ changes by 2ϕ. According to the second Josephson equation,

$$\gamma = (\frac{2\pi}{\phi_0})U, \tag{2.2}$$

this phase leads to a voltage pulse. The area under the pulse, integrated over time, amounts to $\phi_0 \approx 2.07$ mV.ps. Figure 2.2 shows an amplitude against time graph of a single SFQ pulse.

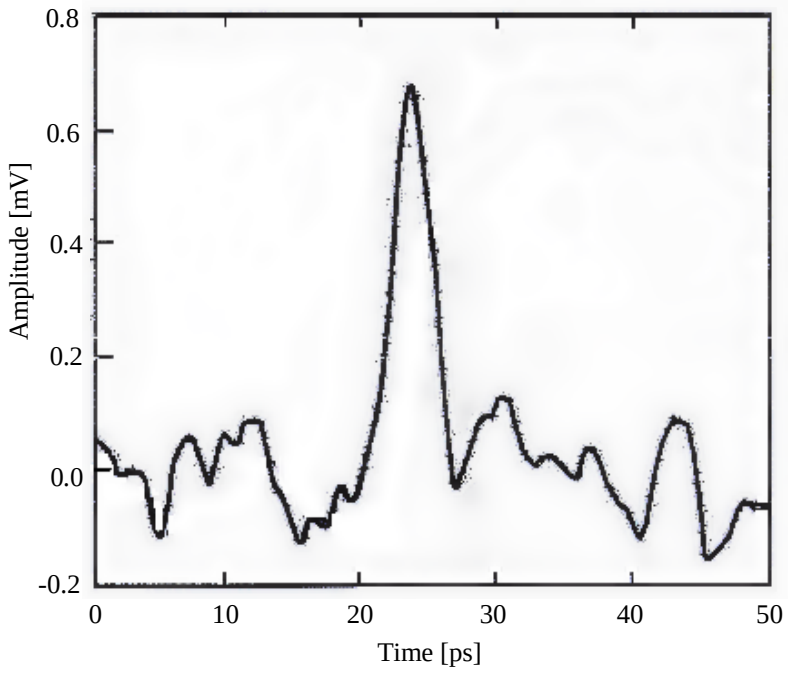


Figure 2.2: Amplitude against time graph of a single SFQ pulse

RSFQ is different from traditional CMOS transistors in the following ways [5]:

- It is based on superconductors, so a cryogenic environment is required.
- Instead of voltage levels, digital signals are represented in picosecond duration pulses. The system is synchronised with a pre-determined clock frequency. If a pulse arrives within a cycle given by the clock, then this corresponds to a 1. If no pulse arrives, this corresponds to a 0.
- The quantum pulses are switched by Josephson junctions.
- Signals cannot be split into multiple outputs without active circuit elements.

RSFQ relies on another intrinsic property of superconductors (apart from the loss of resistance below a critical temperature T_c). Within a closed section of superconducting material any magnetic flux present can exist only in discrete amounts that are multiples of the magnetic flux quantum

$$\Phi_0 = h/2e \approx 2.07 \times 10^{-15} Wb, \tag{2.3}$$

where h is Planck's constant and e is the electron charge [6].

The RSFQ signal was simulated in WRSpice by [7] with a DC-to-RSFQ converter. The RSFQ pulse generator feeds SFQ pulses of a short rise time ($t_r = t_f \approx 10$ ps) and a small voltage amplitude of about 400 μV. The SFQ pulses form a bit pattern with different bit lengths and a clock frequency, $f_{clock} = 100$ MHz.

2.4 Low Temperature Measurements

Operating conditions for RSFQ and Complementary Output Switching Logic (COSL) families are usually inside vacuumed cryocoolers or liquid helium cryostats at cryogenic temperatures. Niobium based RSFQ electronics operate at 4.2 K or below.

Performing measurements at cryogenic temperatures is a very challenging task. Measurements can be done with the use of a cryo dipstick, a temperature measurement control unit, a bottle of liquid helium and various instruments for Direct Current (DC) and Radio Frequency (RF) measurements. Figure 2.3 shows an illustration of a cryo dipstick. At the bottom of the cryo dipstick there is a test chamber in which the DUT is mounted. This chamber is connected by a heat pipe to the liquid helium so that the probe can be cooled down to 4.2 K. A simple resistance within the chamber serves as a heater capable of adjusting to the desired temperature. The actual temperature, measured with a diode, is compared with the temperature required. Real time measurements can be accomplished by connecting the power supply and a pulse generator directly to the cryo dipstick.

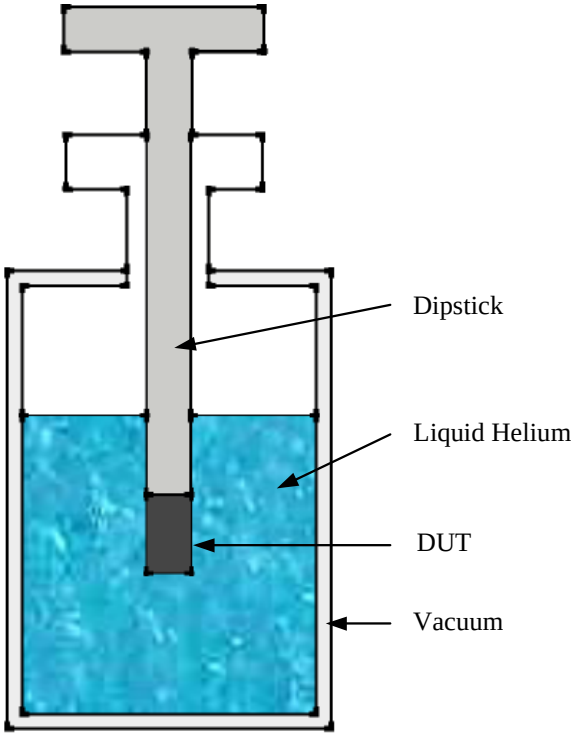


Figure 2.3: Illustration of a Cryo Dipstick.

2.5 Cryorefrigerator

At the University of Stellenbosch a Pulse Tube *Cryomech PT405* cryocooler is used to cool down the DUT. The DUT is enclosed by the cryocooler so it is more distant from the measurement instrument than would normally be the case. A representation of such a cryocooler is given by [8] and reproduced in Fig. 2.4.

A rotary valve in the cold head directs the helium gas in and out of the expansion tubes dropping the temperature to 2.8 K [9]. A first stage is available for shield and lead cooling from 35 to 80 K. The compressor package supplies the cold head with pressurised helium through flexible metal hoses. The DUT is attached to the heat exchanger at the end of the cold head. The heat is then carried to the compressor by the helium where it is discharged into the cooling water.

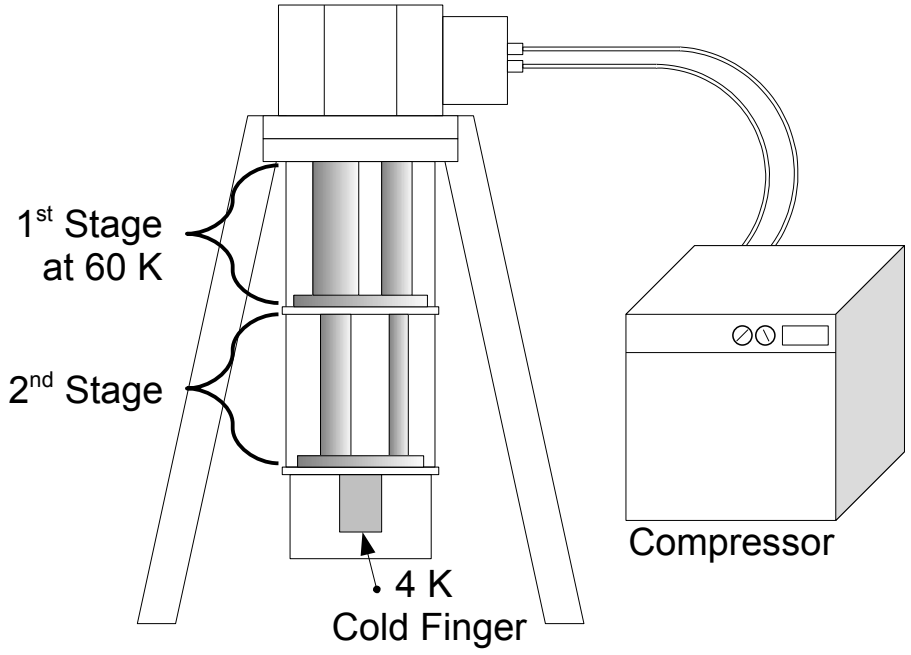


Figure 2.4: Representation of the *Cryomech PT405* cryocooler

The two-stage cryocooler delivers 25 W of cooling power at 65 K and 0.5 W at 4.2 K. Heat sources include electric power dissipation, thermal radiation losses, poorly vacuumed space and heat transferring cables. Multiple thermal shields and a good vacuum (10^{-5} bar), is necessary for reduced heating, but the heat flow through cabling from the outside of the cryocooler still conducts heat into the system. The correct cables should be selected that are sufficient for RF signals and will not conduct too much heat into the system.

The semiconductor electronic devices were tested in the 2^{nd} stage of the cryocooler on the cold finger to get it as close as possible to the actual SCE. The design also needs to be compact in order to fit into the confined space of the 2^{nd} stage. When the amplifier is implemented inside the 2^{nd} stage, the semiconductor electronics is also cooled down to 4 K and the thermal noise on the SCE circuits is significantly less. A theorem by Nyquist [10] states that the mean-square noise voltage appearing across the terminals of a resistor of

$R\ \Omega$ at temperature T Kelvin in a frequency band B hertz is giving by

$$V_{rms}^2 = 4kTRBV^2, \tag{2.4}$$

where k = Boltzmann's constant, relating temperature to energy. Thus, when temperature is reduced, the noise is also reduced thereby creating a more sensitive measurement system.

Measurement accuracy is deteriorated by cable losses and ElectroMagnetic Interference (EMI). EMI could occur due to poor cable shielding [11]. Another aspect is calibration, which is made at room temperature. Cooling down the DUT will change the characteristic of the measurement system. Consequently, appropriate cables must be chosen which have electrical properties independent of temperature. If this is the case, the performed calibration is also valid for measurements at cryogenic temperatures. Care has to be taken that the heat conducted into the cryocooler by the cables does not exceed the heat removal capacity.

2.6 Suzuki Stack Amplifier

Theoretical studies done showed that an RSFQ signal can be amplified with superconducting technology by using a Suzuki stack amplifier [12]. The logic levels of a superconductor circuit are explained in section 2.3. If the superconducting circuit is to be interfaced with the semiconductor circuit, the RSFQ signals must be amplified to drive the semiconductor logic.

The Suzuki stack amplifier is a superconducting digital logic amplifier for interfacing superconductor circuits with semiconductor circuits. It provides a gigahertz amplifier to convert low power superconducting RSFQ signals to higher power signals, suitable for semiconductor signal processing circuits. Figure 2.5 shows the basic schematic of a four stage Suzuki stack amplifier. It provides a factor of four voltage gain to raise the 2.5 mV energy gap across the JJ up to 10 mV. In the same way, a ten stage Suzuki stack amplifier can give a signal of up to 25 mV.

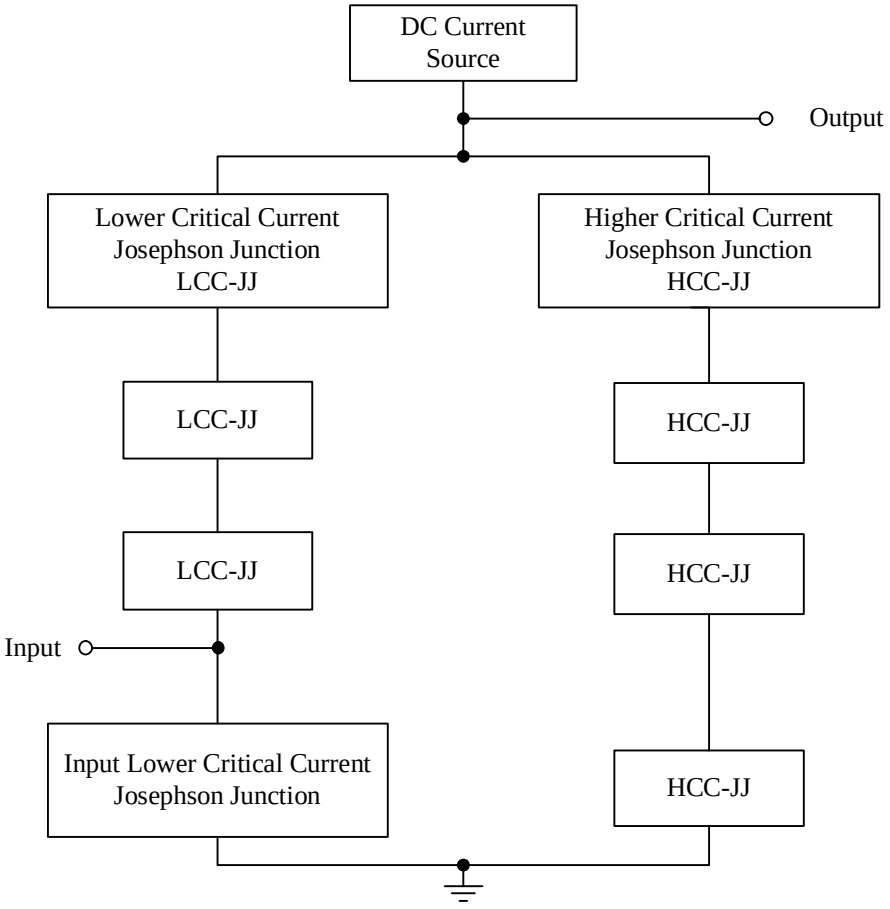


Figure 2.5: Basic configuration of a Suzuki stack amplifier

The amplifier has an input terminal, an output terminal, an input Lower Critical Current Josephson Junction (LCC-JJ) and a first series string of at least three LCC-JJ's. A second series string with at least four Higher Critical Current Josephson Junctions (HCC-JJ) is connected in parallel with the first series string with an upper common connection connected to the output terminal and a pulsed DC current source. The pulsed DC current source controlls the amplifier.

Figure 2.7 shows a voltage against time graph at the input and the output of the amplifier and figure 2.6 shows the current against time graph through

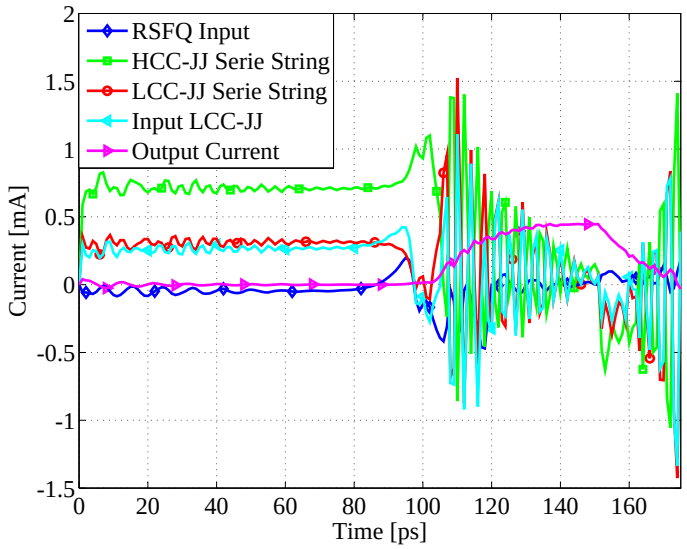


Figure 2.6: Current against time graph in a Suzuki stack amplifier.

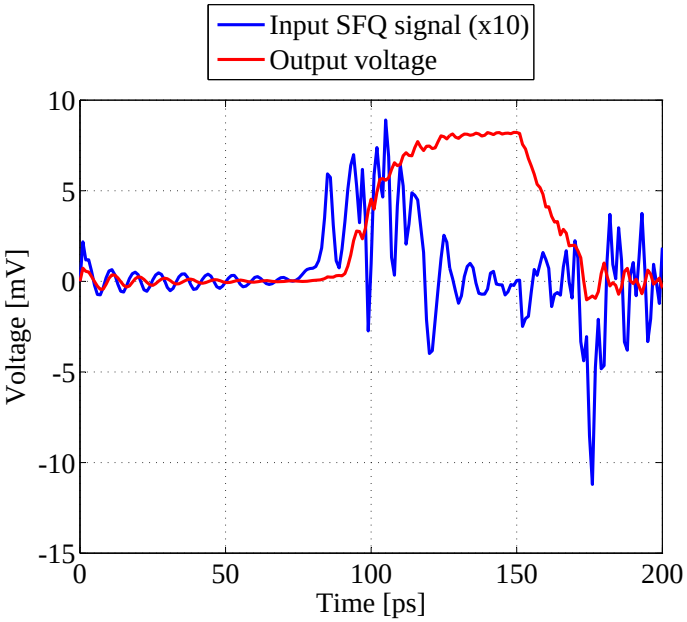


Figure 2.7: Voltage against time graph in a Suzuki stack amplifier.

the input LJJ-CC and the remaining three LJJ-CC's. When the DC current pulse is high, the current is split between the two parallel legs of the amplifier. The critical current of the LCC-JJ's is just higher than the DC current that runs through the first series leg of the LCC-JJ's of the amplifier. When the RSFQ signal is introduced through the input terminal and the DC current pulse is high, the total current through the input LCC-JJ is higher than its critical current and the Junction switch to the resistive state. That forces all the current to run through the second series string of HCC-JJ's.

The critical current of the HCC-JJ's is higher then the DC current that runs through the second series leg of HCC-JJ's, but lower than the total current delivered by the pulsed DC current source. When the input LCC-JJ is switched to the resistive state and all the current runs through the HCC-JJ series string, it switches the HCC-JJ to the resistive state and the current is diverted to the output. That gives an output voltage of the sum of all the energy gap voltages across the JJ's in the series strings. Figure 2.7 shows a voltage against time graph at the input and the output of the amplifier. When the pulsed current source drops, the JJ's returns to their superconducting state. Generally, the Josephson junction portion of the amplifier acts as a latch, being turned on by a signal from the Josephson junction logic circuit and staying on until the end of the pulse from the DC current source.

A ten-stage Suzuki stack amplifier was shown by [12]. The rise time and fall time of the output signal was measured as 10 and 12 picoseconds respectively. They showed that the amplifier can be tuned to operate at 10 GHz by adjusting the frequency of the pulsed DC current source.

It should be noted that ceramic superconductors like Yttrium-Barium-Copper-Oxide (YBCO) can have a ten times larger energy gap than the metallic superconductors like niobium. Thus, with ceramic superconductors, the output of the four stage Suzuki amplifier can be as high as 100 mV.

2.7 DC SQUID Amplifier

A DC SQUID is the most sensitive detector of magnetic flux available [13]. Any physical quantity that can be converted to magnetic flux, e.g., current or magnetic field, can be measured using a SQUID. Although DC SQUID's are inherently capable of amplifying signals at frequencies from DC to a few GHz, [13] showed that the coupling techniques necessary to match the SQUID output signal to room temperature electronics severely limit the usable bandwidth. A transformer or resonant circuit, with Alternating Current (AC) flux modulation and lock-in detection, is usually used to step up the SQUID voltage to the required level. This technique generally limits the bandwidth to tens of kHz, and requires complex room temperature electronics.

Two-stage SQUID amplifiers in which a second SQUID is used to amplify the output of the first have been reported [14]. The gain of the second SQUID is sufficient to make the amplified noise of the first SQUID larger than the intrinsic noise of the second SQUID. A matching transformer is still required at the output of the second SQUID stage to achieve a better low-temperature gain.

Figure 2.8 shows a schematic of the amplifier circuit. It consists of a single input SQUID modulating a 100-SQUID series output array through a 50-turn modulation coil. An input signal I_{sig} couples flux into the input SQUID, which is voltage biased by means of a 25 mΩ resistor so that the SQUID current is modulated by variations in the applied flux. The flux modulation coil of the output array is connected in series with the input SQUID, so that variations in the SQUID current change the flux applied to the output array. The series array is biased at constant current, so the output voltage V_{out} is modulated by this applied flux.

Figure 2.8 shows the input stage consists of a low-inductance double-loop SQUID with a matched input transformer. The two SQUID loops are connected in parallel, with the junctions located between them. The SQUID inductance is therefore half of the individual loop inductance. Two four-turn modulation coils are wound in opposite directions on the SQUID loops

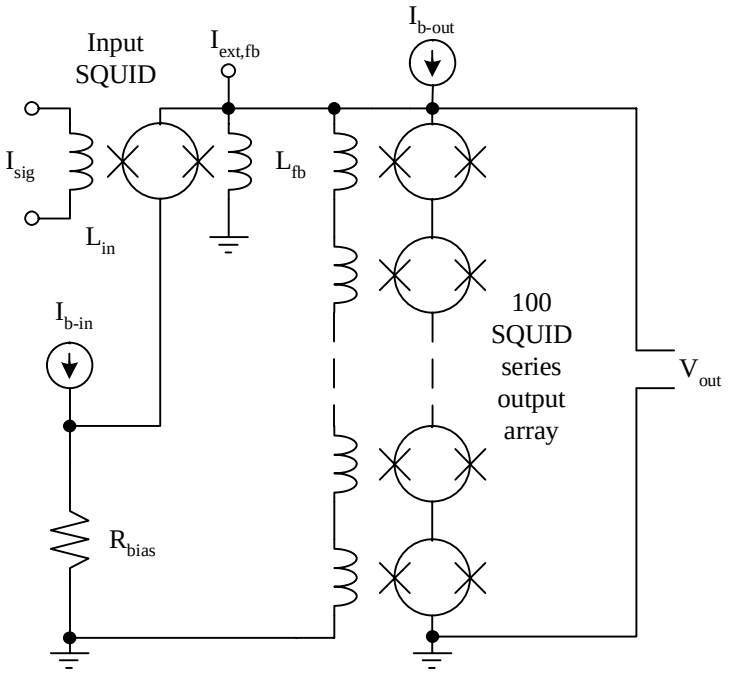


Figure 2.8: Basic configuration of a two-stage SQUID amplifier circuit.

and connected in series. This double coil is connected to the washer of an input transformer. The washer inductance is approximately equal to the input inductance of the modulation coil. While the use of a seperate input transformer results in significant coupling losses compared to a coil wound directly on the SQUID washer, it allows the SQUID inductance to be smaller and helps isolate the SQUID oscillations from input coil resonance.

The gain required from the output stage is determined by the amplitude of the input SQUID current noise and the desired amplitude of the output voltage noise. The gain of the amplifier is proportional to $N_{sq}N_t$, where N_{sq} is the number of SQUID's in the series array and N_t is the number of turns in its modulation coil. Increasing N_{sq} linearly increases the maximum output voltage swing ΔV_{out}, and hence the gain, since the SQUID's in the array are modulated coherently. The noise in the array increases only as $\sqrt{N_{sq}}$, but since the noise voltages are expected to add incoherently, the total output noise of the amplifier is dominated by the amplified noise of the input stage.

N_{sq} and N_t may be chosen to maximise the bandwidth and the dynamic range. The bandwidth of the two-stage amplifier is determined by the lowest cut-off frequency in the system,

$$f_c = R_{dyn}/2\Pi L_{in}, \tag{2.5}$$

where R_{dyn} is the dynamic resistance of the input SQUID and L_{in} is the input inductance of the output array modulation coil. This input inductance is proportional to ${N_t}^2 N_{sq} L_{sq}$, where L_{sq} is the inductance of a single SQUID in the output array. Since L_{in} increases more rapidly with N_t than with N_{sq}, it is best to achieve the required gain by increasing N_{sq} rather than N_t. Increasing N_{sq} maximises the dynamic range since ΔV_{out} increases.

A 100-SQUID series array with an input transformer with 36 primary turns was shown by [15] to have a bandwidth of at least 175 MHz when operated alone.

2.8 CMOS Amplifiers

A CMOS amplifier is needed that can operate at 4.2 K. Several advantages are shown by [1] in CMOS devices operating at low temperatures. First the carrier mobility is increased due to decreased lattice scattering at low temperatures, resulting in the enhancement of device current and switching speed. The junction capacitances are also reduced at low temperatures due to carrier freeze-out. For the same reason, leakage currents decrease exponentially with decreasing temperature. This results in the reduced sub-threshold coefficient α and an increase in the threshold voltage, which suggests a very small voltage operation is feasible with careful adjustment of threshold voltages. The threshold voltage variation is symmetrical, and consequently CMOS logic has a very wide temperature range of operation. This suggests that CMOS circuits for low-temperature operation can be adjusted and matched at room temperature.

Field effect mobility was measured by [1] from transconductance at low drain voltages. In the long-channel case, the increase was about a factor of six larger for liquid nitrogen temperatures (77 K) compared to room temperature measurements, while a factor of eight was observed at liquid helium temperatures (4.2 K). However, for the short-channel case, the mobility increase appears to be smaller than in the long-channel case.

Figure 2.9 shows the subthreshold current characteristics of the Metal Oxide Semiconductor (MOS) transistor pair tested by [1]. The current-voltages characteristics showed that a lowering in the temperature meant the channel conductance of both transistors would increase very symmetrically. This means that the proper design ratio can be maintained even at cryogenic temperatures. It can be seen from a practical viewpoint that with cooling down, there is a great beneficial effect on the transconductance (g_m) increase.

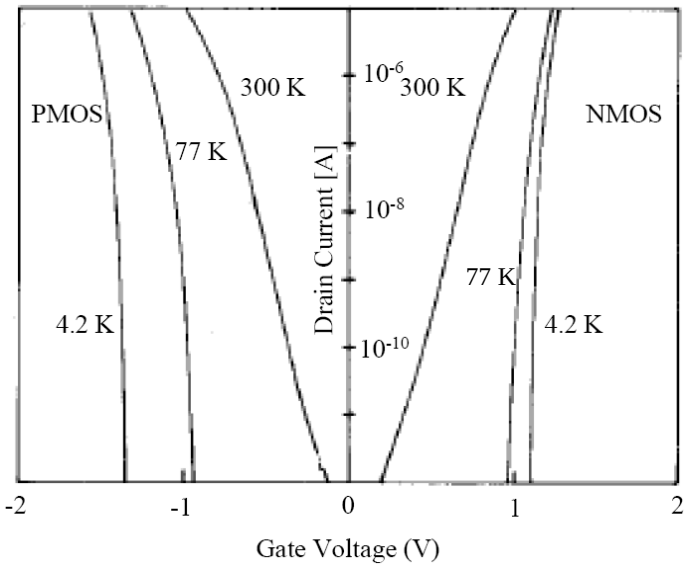


Figure 2.9: Subthreshold current characteristics as cited in [1].

Figure 2.10 shows the cross section of a CMOS transistor. Variations in sheet resistances was tested by [1].

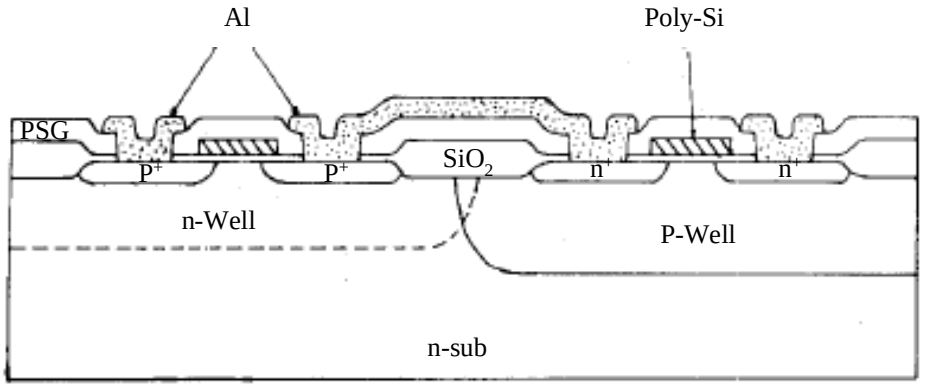


Figure 2.10: Cross section of a CMOS transistor pair as cited in [1].

Figure 2.11 shows the variations of the sheet resistances for polysilicon, p^+- and n^+-type diffusion layers as well as p-Well and Aluminium (Al) metals with decreasing temperature. In low impurity concentration situations, such as p-Well, the resistivity decreases due to an increase of mobility down to 77 K. However, carrier freeze-out causes a steep increase in p-Well resistivity at 4.2 K. The p-Well resistance increases above 10^{10} ohm/square. at 4.2 K. [1]

Other resistance drop with decreasing temperature down to 4.2 K. In particular, Aluminium metal resistance drops drastically because of reduced lattice vibrations. This gives a great advantage to reducing noise caused by CMOS switching and power supply line resistance.

The gate capacitance (C_G) and junction capacitance (C_j) was measured by [2]. They found that the capacitance decreases with decrease in temperature in the depletion region ($V_G < 0$ V), while there is almost no temperature dependence in the inversion region ($V_G > 0$ V). The reduction of C_G in the depletion region is due to the carrier freeze-out effect, which means that all extra electrons and holes are captured by their dopant atoms. In the inverse region the extra electrons are provided from the heavily doped source

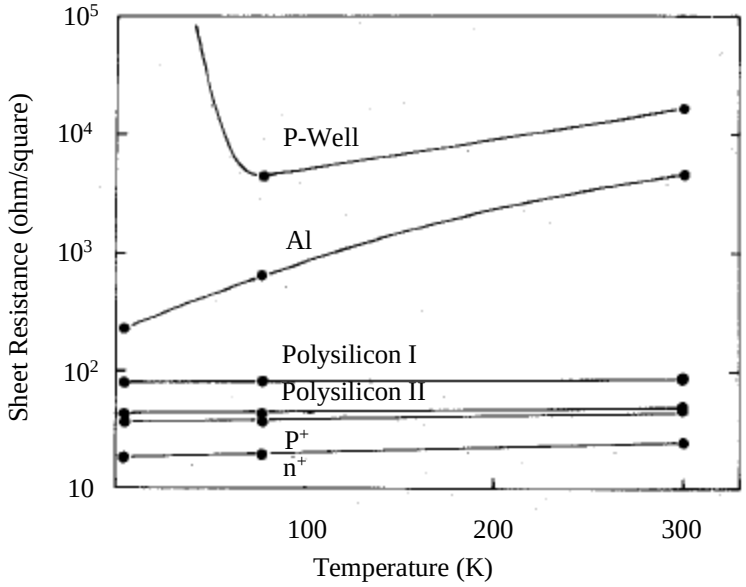


Figure 2.11: Variations of sheet resistances for polysilicon, p^+-, and n^+-type diffusion layers, as well as p-Well and Al metals with decreasing temperature as measured by [1].

and drain regions nearby, resulting in the simple parallel plate capacitance between the gate and channel. At 300 K, C_j decreases with increase in reverse junction voltage. At 4.2 K, however, C_j drops by about a factor of ten because of carrier freeze-out in the substrate.

An n-p-n Bi-CMOS transistor with a p^+ injector was also measured by [1] to plot the latch-up behaviour at low temperatures of the BiCMOS devices. BiCMOS refers to the integration of bipolar junction transistors and CMOS technology into a single device. The base current was injected from the p^+ layer to the p-Well. The current at which latch-up was observed was calculated as a function of temperature. Figure 2.12 shows the latch-up base current increases with a decrease in temperature. The current gain for the n-p-n at room temperature was 230. That went down to 4 at 77 K and to 0.4 at 4.2 K. Therefore a bipolar-CMOS configuration will not work below 100 K. Practically speaking, no latch-up was observed at temperatures below 100 K.

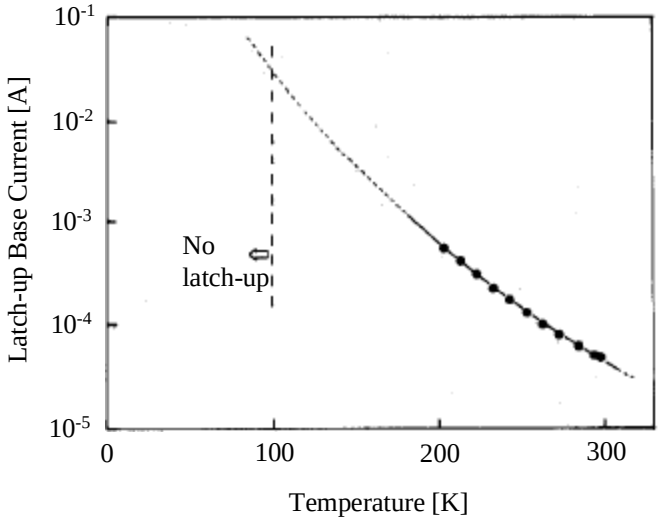


Figure 2.12: Latch-up base current versus temperature

2.8.1 350 nm Channel Length or Smaller

Experiments done by [2] showed characterisation and modelling of CMOS devices at 4.2 K. The CMOS devices examined in that study are commercially available short-channel devices with channel lengths of 0.18 μm, 0.25 μm and 0.35 μm. They developed a short-delay CMOS amplifier which would amplify a 40 mV voltage input to CMOS voltage levels (1 V) with a propagation delay of 104 ps, with the use of a 0.18 μm CMOS process. A substantial reduction of the sub-threshold slope was observed at low temperatures, which was evaluated to be 100 mV/dec, 25 mV/dec and 20 mV/dec at 300 K, 77 K and 4.2 K respectively for the 0.35 μm device.

The propagation delay of a 0.35 μm CMOS inverter was measured by using a ring oscillator [2]. They used oscillation frequencies of three ring oscillators with different numbers of inverter stages to get the single-inverter delay. Figure 2.13 shows the dependence of the propagation delay of the inverter on the supply voltage at 300 K and 4.2 K [2]. The experimental results indicated about 40% speed up from 300 K to 4.2 K.

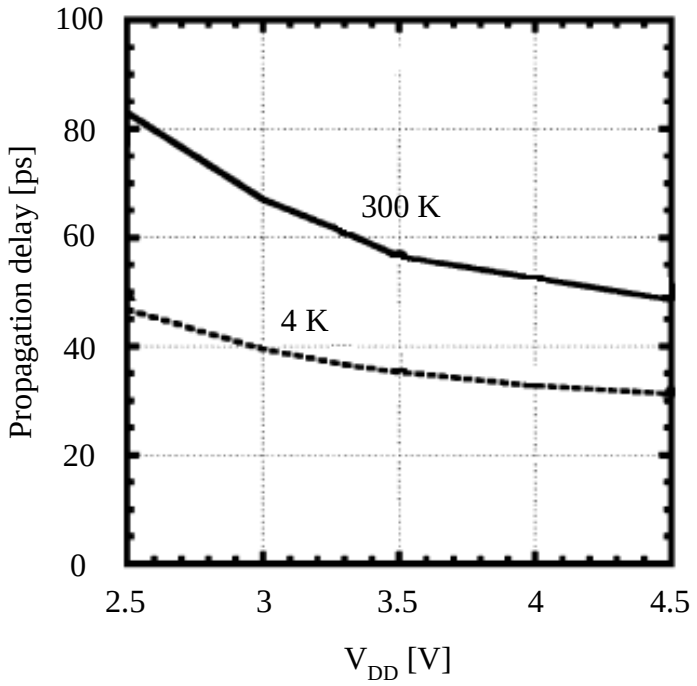


Figure 2.13: Dependence of the propagation delay of a CMOS inverter fabricated by a 0.35 μm CMOS process on the supply voltage at 300 K and 4 K [2].

Based on these results, they estimated the power dissipation of the CMOS transistor at 4.2 K. The power consumption of the CMOS circuit was calculated with,

$$P = C_L V_{DD}^2 f, \tag{2.6}$$

where C_L is the total load capacitance, f is the clock frequency and V_{DD} is the positive supply voltage. From figure 2.13, one can calculate a maximum improvement. When V_{DD} is reduced with 20 % (from 3.5 V to 2.8 V), the propagation delay increases with /mbox30 %. Thus the clock frequency also increases with 30 %. C_L is composed of C_G, C_j and the wiring capacitance. Because the wiring capacitance and C_j are reduced substantially at low temperature, they measured a 50% reduction of C_L at cryogenic temperatures. Putting all the values into eq 2.6, shows that a 60% reduction in the power consumption is expected at 4.2 K.

2.8.2 Hi-CMOS Technology

Further experiments were done by [1]. The paper reports on low-power consumption high-speed operation of bulk CMOS devices at 77 K and 4.2 K. The samples were fabricated using the Hi-CMOS II process which has been applied to several practical large scale integration (LSI) circuits.

The n-channel MOS transistor is formed in a p-Well and the source-drain diffusion layers are made through arsenic and phosphorus double implants. P-channel devices are formed in an n-Well and the source drain diffusion layers are made by boron implantation. Both of these transistors have n^+ -doped polysilicon gates with a gate length of 2 μm. The gate oxide thickness is 35 nm. The substrate is 10 Ω.cm n-type. Throughout their experiments, surface ohmic contacts were used both in the p-Well and n-Well to stabilise the potential. The chips were diced and mounted on dual in-line ceramic packages with no package seals. Measurements of electrical characteristics were made using samples immersed directly into liquid nitrogen (77 K) or liquid helium (4.2 K).

They found that with cooling down of the Hi-CMOS II circuit, the power dissipation decreased by up to 20%, while the propagation delay decreased by up to 40%. The propagation delay indicates a useful improvement between 77 K and 4.2 K, while MOS characteristics do not change appreciably.

Hi-CMOS III technology is explained by [16]. It is the 2/3 scaling of Hi-CMOS II with constant voltage, Lightly Doped Drain (LDD) N-type Metal Oxide Semiconductor (NMOS) and newly developed Buried Channel Lightly Doped Drain (BCLDD) P-type Metal Oxide Semiconductor (PMOS), with polycite gate area adopted to reduce short channel effects and delays in interconnection lines. Post-contact doping was also adopted to allow the overlap of contact holes and diffusion edges and to reduce contact resistance.

Hi-CMOS III main features are summarised in Table 2-I and compared with Hi-CMOS I and Hi-CMOS II.

Table 2-I: The evolution of Hi-CMOS technology

	Hi-CMOS I	**Hi-CMOS II**	**Hi-CMOS III**
Supply Voltage [V]	5	5	5
Gate length [μm]	3.0	2.0	1.2
NMOS structure	Phos. Dif.	Graded Drain	LDD
PMOS structure	Boron Dif.	Boron Dif	BCLDD
Gate oxide thickness [nm]	50	35	25
Field oxide thickness [nm]	650	650	650
Junction depth N-layer [μm]	0.50	0.35	0.25
Junction depth P-layer [μm]	0.50	0.40	0.40
Gate (width/space) [μm]	3.0/3.0	2.0/2.0	1.2/1.4
Al (width/space) [μm]	3.0/4.0	3.0/2.0	1.3/1.6
Contact hole [μm]	3.5	2.0	1.2
Saturation current NMOS [A/m]	107	164	255
Saturation current PMOS [A/m]	49	72	118
NMOS BVds [V]	10.5	9	9.5

2.8.3 p-HEMT

In general, to allow conduction, semiconductors need to be doped with impurities to generate mobile electrons in the layer. This causes electrons to slow down because they end up colliding with the impurities which were used to generate them in the first place. HEMT (High Electron Mobility Transistor), however, is a smart device to resolve this seemingly inherent unsolved contradiction.

Figure 2.14 shows the cross section of a AlGaAs/GaAs p-HEMT. HEMT is explained by [17]. It is a field transistor with a junction between two materials with different bandgaps as the channel instead of a doped region. A commonly used combination is GaAs (Gallium Arsenide) with AlGaAs (Aluminium Gallium Arsenide). It use high mobility electrons generated using the heterojunction of a highly-doped wide-bandgap n-type donor-supply layer (AlGaAs) and a non-doped narrow bandgap channel layer with no dopant impurities (GaAs). The heterojunction created by the different bandgap materials forms a quantum well in the conduction band on the GaAs side.

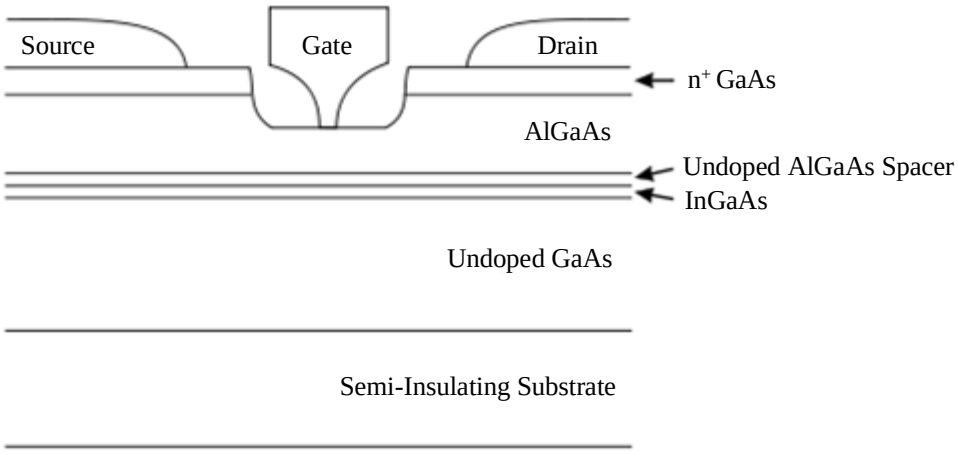


Figure 2.14: Cross section of a AlGaAs/GaAs p-HEMT

That forces the electrons generated in the n-type AlGaAS thin layer to drop completely into the GaAs layer to form a depletion AlGaAs layer. The electrons can move fast in the GaAs side without colliding with any impurities bacause the GaAs layer is undoped. That creates a very thin layer of highly mobile conducting electrons , giving the channel very low resistivity and high electron mobility. This layer is called a two-dimensional electron gas. As with all other FET's (Field-Effect Transistors), a voltage applied to the gate alters the conductivity of the layer.

Ordinarily, the two different materials used for a heterojunction must have the same lattice constant (spacing between the atoms). A p-HEMT (pseudomorphic HEMT), however, has a different lattice constant for the two different materials. This feat is achieved by using an extremely thin layer InGaAs (Indium Gallium Arsenide). The layer is so thin that the crystal lattice simply stretches to fit the other material. This technique allows the construction of transistors with larger bandap differences than otherwise possible for better performance.

Various hybrid amplifiers based on commercially available p-HEMT transistors in a embedded microwave design were designed and characterised by [18]. They demonstrated the functionality of hybrid p-HEMT amplifiers for

cryogenic applications and successfully tested its digital operations at 4.2 K. They achieved a total power consumption of less than 10 mW and a voltage gain of about 30 dB at 4.2K.

2.9 Cryogenic behaviour of resistors and capacitors

The complete amplifier should work at 4.2 K, therefore each component type should be tested separately to confirm correct functionality at the specified temperature.

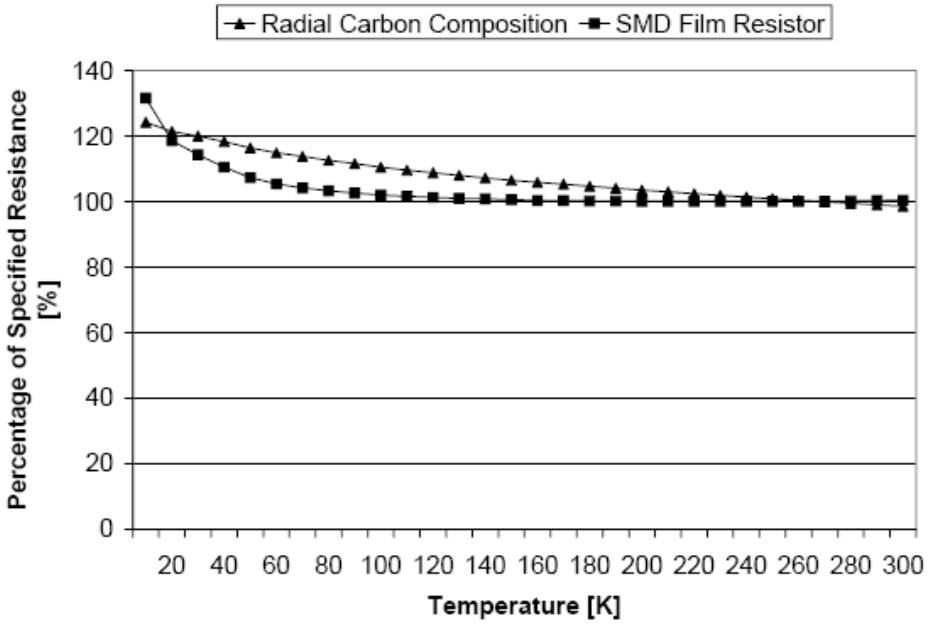


Figure 2.15: Tested resistor types with characteristic plots against cryogenic temperature range

Two types of resistors were tested by [19]. One is a radial carbon composition resistor and the other a 0.25 watt Surface Mount Device (SMD) carbon film resistor. Figure 2.15 shows their characteristics over a wide temperature range, from 10 K to 300 K. From the graph it can be noted that the SMD

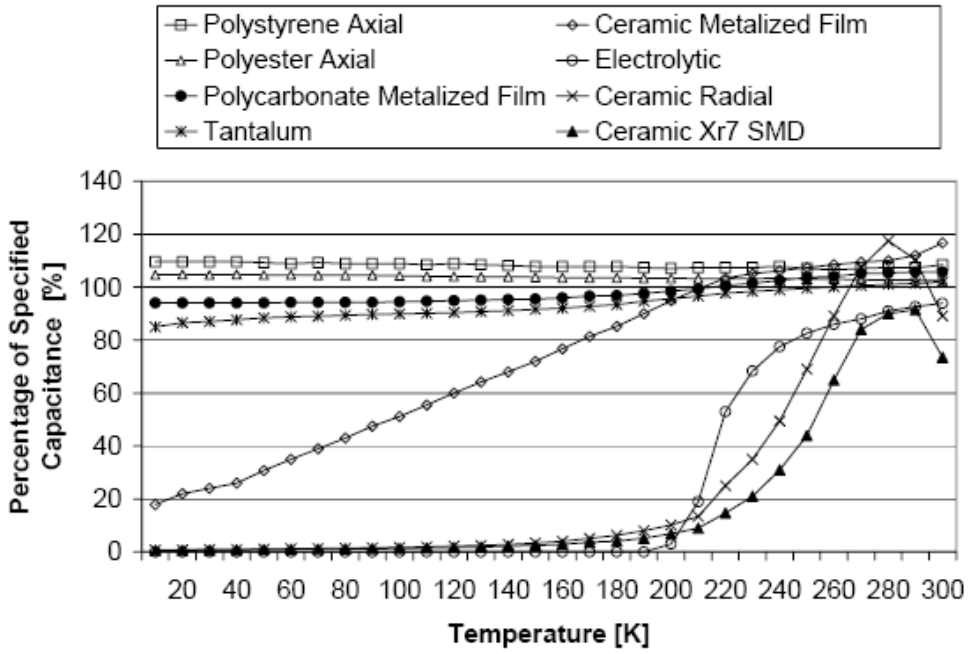


Figure 2.16: Tested capacitor types with characteristic plots against cryogenic temperature range

carbon film resistors had a 30 % increase in resistivity, while the radial carbon composition resistors had an increase of 22 %. In this design the SMD carbon film resistor is preferred above the radial carbon composition resistors because it is manufactured in SMD package types which take up less space. It is mainly used as feedback, gain and matching resistors, the change in the resistivity can be incorporated into the design.

Figure 2.16 shows eight different types of capacitors that were tested by [19] inside the cryocooler. Their results indicated that the polystyrene, polyester, polycarbonate and tantalum capacitor types have an acceptable performance with a less than 20 % deviance. The capacitors is mainly used as decoupling capacitors that do not require precision capacitor values.

Chapter 3

Design Overview

This thesis consists of two parts. The first deals with the SCE, which consists mainly of a Suzuki stack amplifier. It would amplify the power of each SFQ pulse by increasing its amplitude and width. The SCE was not manufactured, but simulation results are provided.

The second deals with the low temperature (4 K) behaviour of commercially available CMOS amplifier IC's. Section 3.2 shows the design of a test setup used to characterise these amplifiers.

3.1 SCE Design Considerations

The SCE will only be simulated in WRSpice [20] and a circuit layout will be done in Lasi 6. The Hypres design rules [21] were followed and a Monte Carlo analysis was performed with Hypres manufacturing tolerances.

Any superconducting strip that connects two components has an inductance. This inductance is very important in SCE's [22]. Inductance in microstrip lines cannot be described in terms of the line length alone. Different programs, such as Lmeter [23], may be used to calculate inductances in the SCE structures.

For the simulations, an inductance of at least 0.13 pH was used between all the connections in the circuit. That would account for the inductance of the superconducting strip connecting the components. A larger inductance was used (calculated using Lmeter) for a longer connection.

3.1.1 SCE Block Diagram

A block diagram of the SCE is presented in figure 3.1. It starts with three square voltage pulses with a width of 60 ps and amplitude $V_1 = 0.4$ V. A resistor (R_1) must be included to limit the current so that the DC-to-SFQ converter receives a maximum current of 1500 μA [7]. For an input voltage of 0.4 V, R_1 was calculated to be 278 Ω. The first pulse would start after 60 ps, the second pulse after 360 ps and the last pulse after 940 ps. That would simulate a 1101 digital RSFQ signal synchronised with the 3.33 GHz clock signal of the Suzuki stack amplifier. The frequency of the clock signal was randomly selected to have a frequency of 3.33 GHz and a period of 300 ps.

The block pulse is converted into a SFQ signal with a DC-to-SFQ converter adapted from [7]. The SFQ signal goes through a 250 μA Josephson Transmission Line (JTL). A JTL is a standard for RSFQ circuits to ensure circuit interconnection compatibility. For the 1 kA/cm^2 process from Hypres, a JTL with 250 μA junctions was chosen as standard [7]. The JTL delays the SFQ signal with 14 ps. A current block prevents the current from the Suzuki amplifier to interfere with the SFQ signal. The Suzuki amplifier together with its block diagram was explained in section 2.6. The SCE would have a digital 1101 output signal synchronised with a 3.33 GHz clock signal.

Figure 3.2 shows the complete circuit layout of the SCE. Section 3.1.2 up to section 3.1.4 explains the different building blocks of the SCE. The complete circuit was simulated and measurements of the different building blocks were done while part of the complete system.

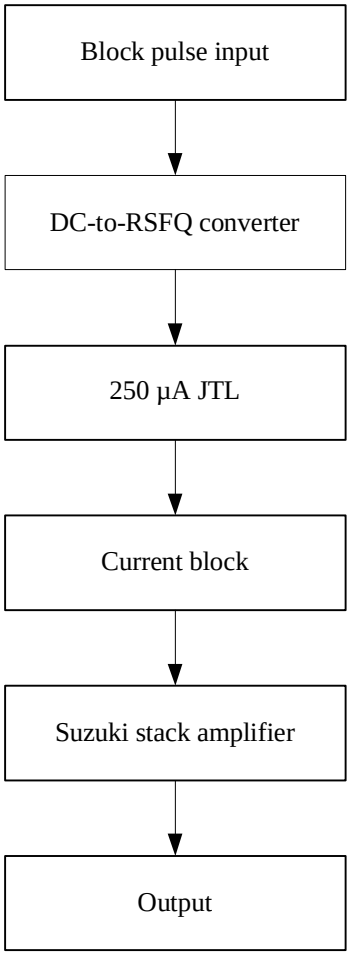


Figure 3.1: Block diagram of the SCE.

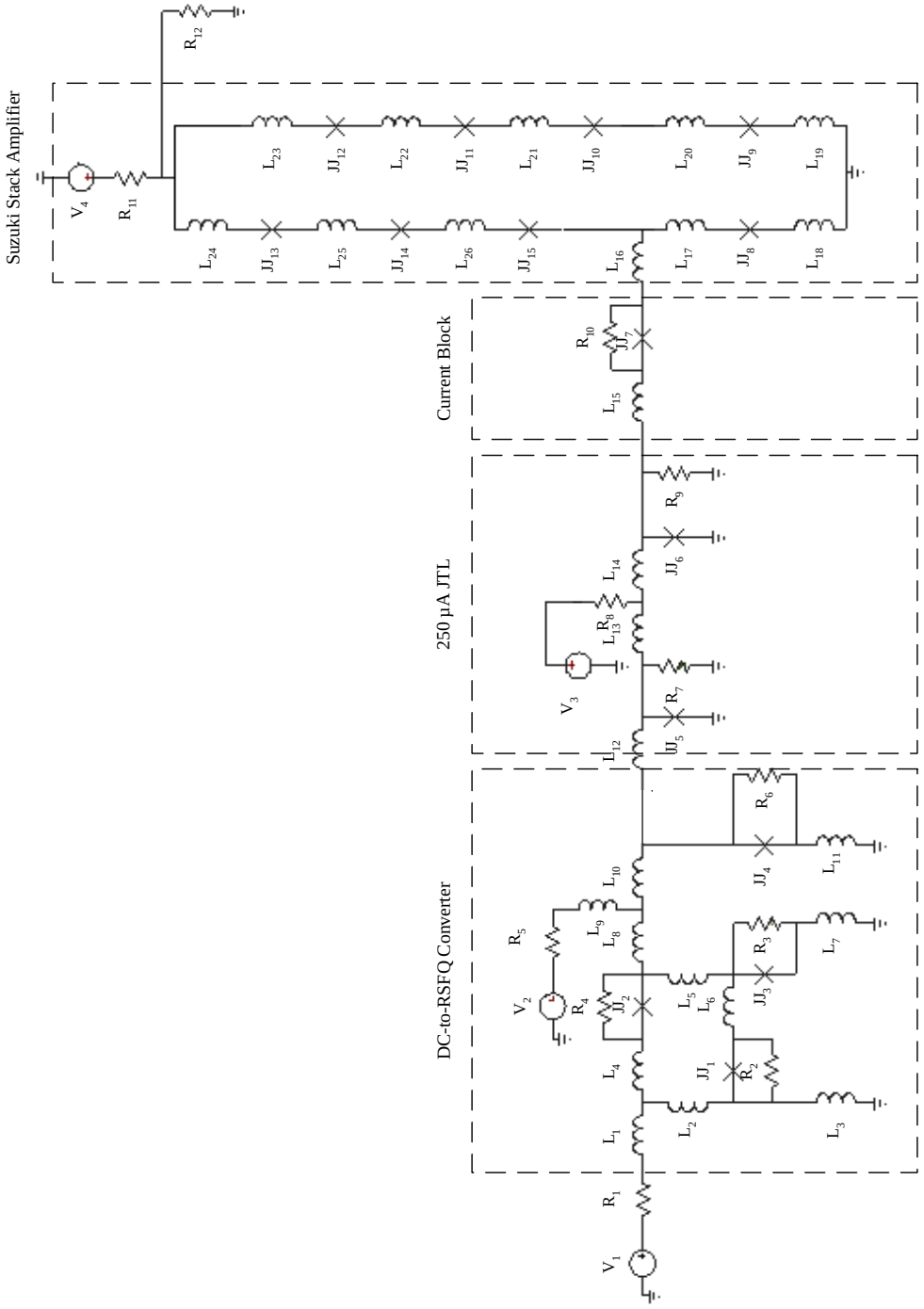
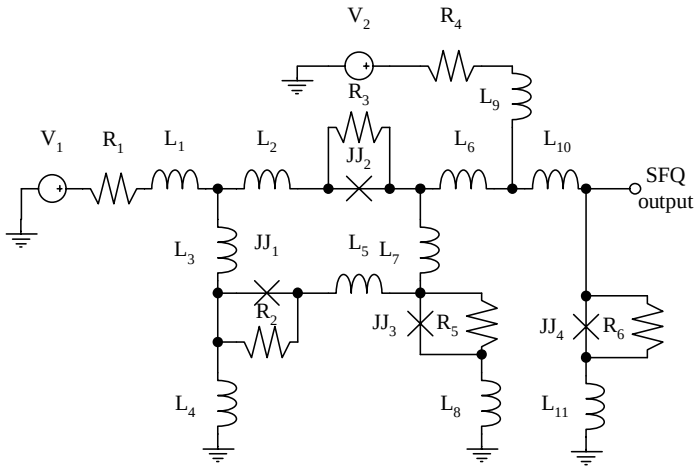


Figure 3.2: Full circuit layout of the SCE.

3.1.2 DC-to-SFQ Converter Circuit Layout

Figure 3.3 shows the circuit layout of the DC-to-SFQ converted adapted from [7]. R_1 was calculated to be 278 Ω for the DC-to-SFQ converter to receive no more than 1500 μA. The transmission strip connection inductances were calculated by [7]. The circuit is biased with V_2 = 2.6 mV and a resistor R_4 = 6.4 Ω to give a current bias of 400 μA. The objective, according to [7], is to cancel the effect of global tolerances on the current bias of grounded JJ's. A global increase in resistance leads to a directly proportional reduction in the bias current of each junction. That can be counteracted if the DC bias voltage is increased by the same proportion.

The Hypres process specifies a junction through 1 kA/cm² or 10 μA/μm². That means in the layout only the area of the JJ will be a variable. A JJ with a I_c of 250 μA will thus have an area of 25 μm². The Josephson Junctions JJ_1 to JJ_4 were damped with parallel resistors. Junction damping resistors were automatically adjusted after every junction area alternation in order to set their Stewart-McCumber parameters equal to 1 [7].



Component	Value
R_1	278 Ω
R_2	2.05 Ω
R_3	1.78 Ω
R_4	6.4 Ω
R_5	1.78 Ω
R_6	1.24 Ω
JJ_1	148 μA
JJ_2	171 μA
JJ_3	171 μA
JJ_4	245 μA
L_1	10 pH
L_2	1.29 pH
L_3	1.27 pH
L_4	3.6 pH
L_5	0.7 pH
L_6	1.13 pH
L_7	0.29 pH
L_8	0.13 pH
L_9	10 pH
L_{10}	1.74 pH
L_{11}	0.13 pH

Figure 3.3: Circuit layout of the DC-to-SFQ converter.

They used the equation

$$\beta_c = \frac{2e}{h} I_c R_{ef}^2 C \tag{3.1}$$

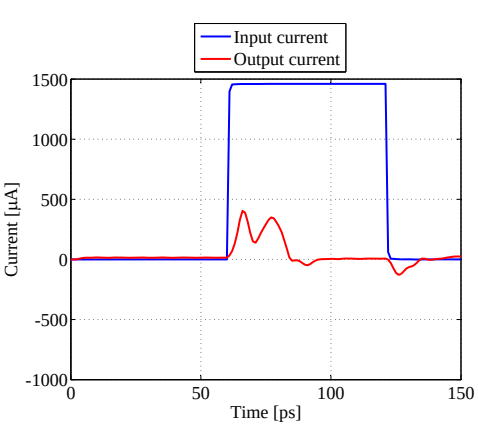
with

$$R_{ef}^{-1} = R_n^{-1} + R_s^{-1}, \tag{3.2}$$

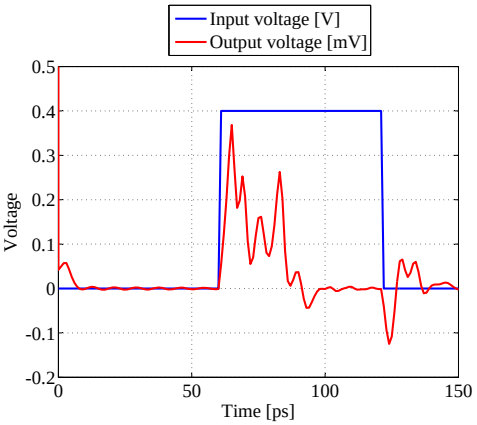
where R_n is the normal resistance of the JJ and R_s the impedance of the environment connected to the junction. For RSFQ $\beta_c = 1$, e is the electron charge, h is Planck's constant, I_c the critical current of the junction and C the capacitance.

Figure 3.4 shows the graph of the input and output current and voltage of the DC-to-SFQ converter. Figure 3.2 on page 31 shows the complete system. The input was measured as the signal delivered by V_1 and the output was measured before the inductor L_{12}. The DC-to-SFQ converter takes a rising edge and converts it into an SFQ signal. The converter produces either a single SFQ pulse per period of the input block signal, or two SFQ pulses per period depending on the amplitude of the block signal [24].

Due to the nature of SFQ pulses and the speed of conversion of a DC-to-SFQ converter, input voltage pulses need only stay high for a few picoseconds [7].



(a) Input and output current against time graph.

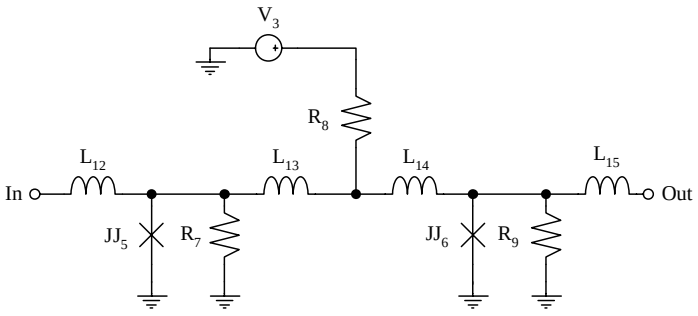


(b) Input and output voltage against time graph.

Figure 3.4: Time analysis of the input and output signals of the DC-to-SFQ converter.

3.1.3 JTL250 Circuit Layout

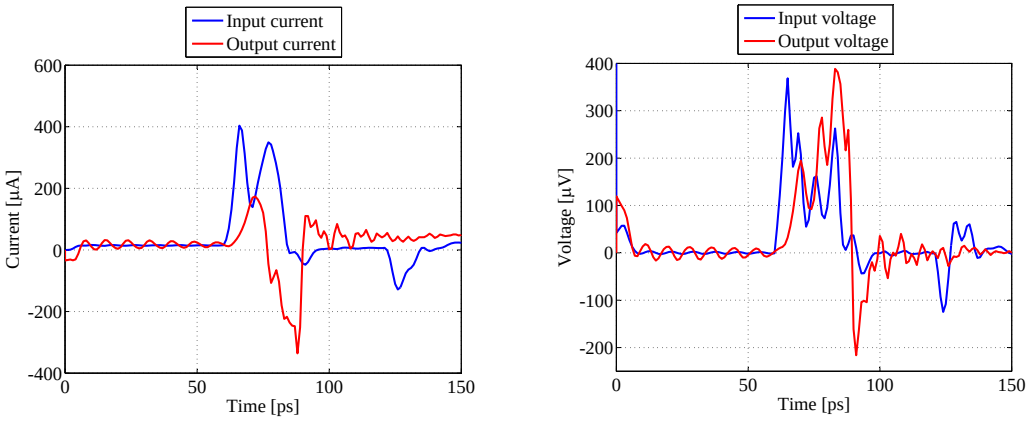
Figure 3.5 shows the circuit layout of the 250 μA JTL [7]. The layout structure was designed to have an inter-junction inductance of 4 pH. The Josephson Junctions are damped with parallel resistors and the circuit is biased with $V_3 = 2.6$ mV and a resistor $R_9 = 15.6\ \Omega$ to provide a current bias of 167 μA.



Component	Value
R_7	1.22 Ω
R_8	1.22 Ω
R_9	15.6 Ω
L_{12}	2 pH
L_{13}	2 pH
L_{14}	2 pH
L_{15}	2 pH
JJ_5	250 μA
JJ_6	250 μA

Figure 3.5: Circuit layout of the JTL250.

The input and output of the JTL was measured while connected to the complete system. Figure 3.2 on page 31 shows the JTL as part of the complete system. The input was measured before the inductor, L_{12} and the output was measured after the inductor, L_{15}. Figure 3.6 shows the graph of the input and output current and voltage through the 250 μA JTL. The JTL decreases the total current of the SFQ pulse, but increases its voltage. It gives the SFQ signal a delay of 16 ps.



(a) Input and output current against time graph.

(b) Input and output voltage against time graph.

Figure 3.6: Time analysis of the input and output signals of the 250 μA JTL.

3.1.4 Current Block

A Josephson Junction is used to prevent the current that drives the Suzuki stack amplifier from interfering with the rest of the circuit. Figure 3.2 on page 31 shows the current block in the complete system. The Josephson Junction, JJ_7, has an I_c of 194 μA, which is damped with a parallel resistor R_{10} with a resistance of 2 Ω. The Josephson Junction is connected in series with the circuit, after the JTL before the input for the Suzuki stack amplifier, and have no influence on the current. Figure 3.7 shows an increase, from 400 μV to 600 μV, in the peak voltage of the SFQ signal.

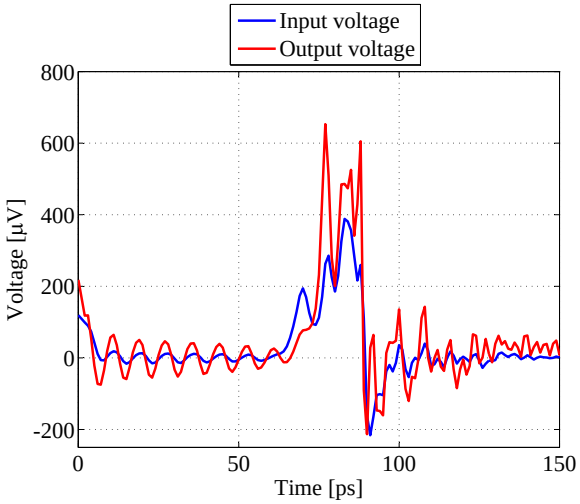


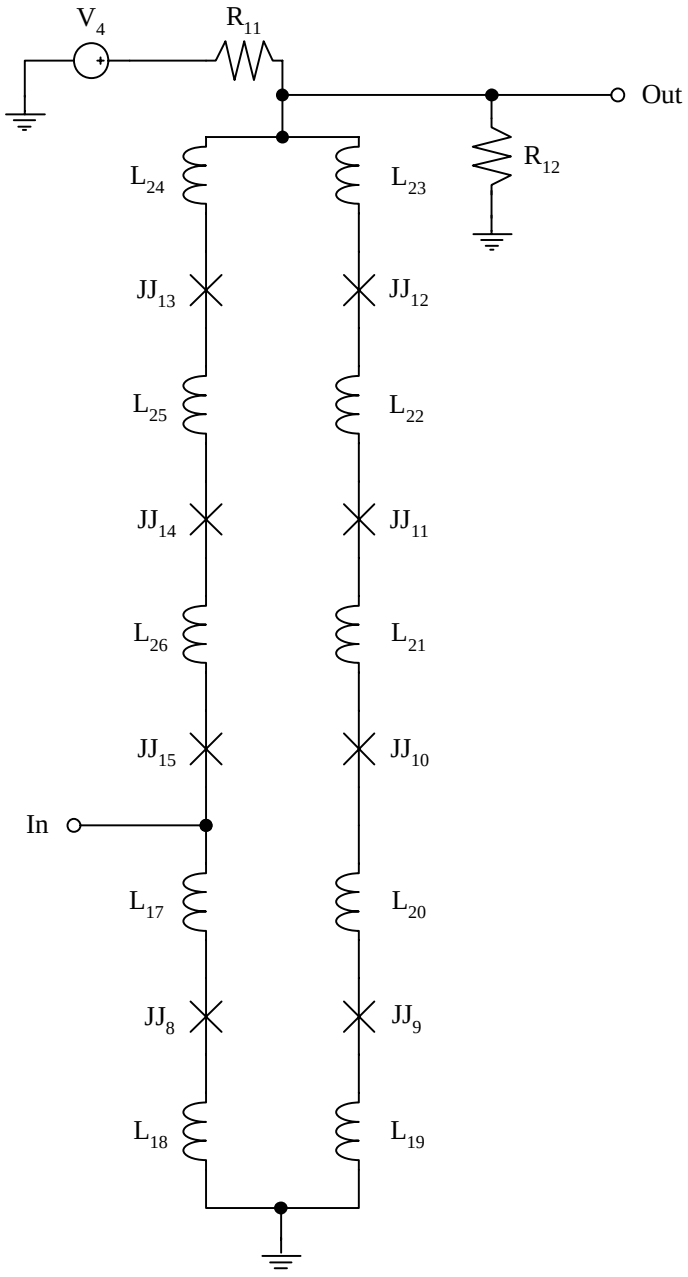
Figure 3.7: Time analysis of the voltage through the current block.

3.1.5 Suzuki Stack Amplifier Circuit Layout

Figure 3.8 shows the circuit layout of the Suzuki stack amplifier. The amplifier is synchronised by a clock signal (V_4). V_4 is a block signal with an amplitude of 20 mV and a frequency of 3.33 GHz. It is fed through a resistor ($R_{11} = 19.55\ \Omega$). That gives the Suzuki stack amplifier a clock signal with a current of 1.023 mA. Due to the inductive differences of the two parallel legs, the current splits through the two parallel legs when the signal is high. The current is split into 351 μA through the LCC-Josephson Junction leg and 672 μA through the HCC-Josephson Junction leg (see section 2.6).

The LCC-Josephson Junctions (JJ_8, JJ_{13}, JJ_{14} and JJ_{15}) have a I_c just higher than the current through the LCC-Josephson Junction leg. The I_c must be close enough to the current through the leg for the SFQ signal to switch the junction, but not too close for the noise to switch the junction. Their critical currents was chosen to be 450 μA.

The HCC-Josephson Junctions (JJ_9 to JJ_{12}) have a I_c higher than the current through the HCC-Josephson Junction leg of the amplifier, but lower than the total current produced by V_4. Their critical current was chosen to be 1 mA. This value is high enough to prevent the noise in the system to switch the



Component	Value
R_{11}	19.55 Ω
R_{12}	18.4 Ω
L_{17}	0.13 pH
L_{18}	0.29 pH
L_{19} to L_{26}	0.13 pH
JJ_8	450 μA
JJ_{13} to JJ_{15}	450 μA
JJ_9 to JJ_{12}	1000 μA

Figure 3.8: Circuit layout of the Suzuki stack amplifier.

Josephson Junctions, but still lower than the total current delivered from the external source.

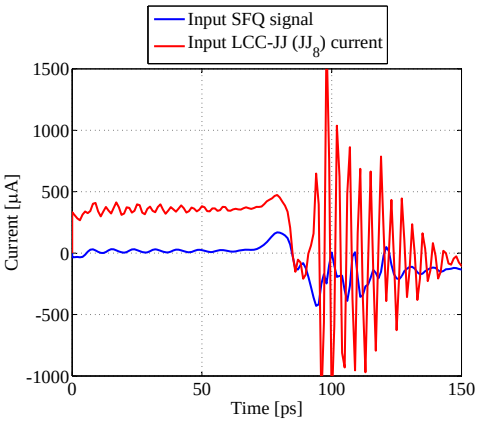
The amplitude of the clock signal (V_4) when it is high, much reach a value of between 19.7 mV and 20.3 mV when it receives the SFQ signal. If the amplitude of V_4 is smaller than 18.5 mV, the SFQ signal will not switch the input LCC-Josephson Junction (JJ_8) to its resistive state. If V_4 reach an amplitude of more than 21.5 mV, the noise in the system will be enough to switch JJ_8.

The connections between the Josephson Junctions was simulated by inductors with inductance of 0.13 pH. A larger inductance (L_{18} = 0.29 pH) was used to give the inductive difference between the two parallel legs of the amplifier. The output of the signal is delivered to a load resistor (R_{12} = 18.5 Ω).

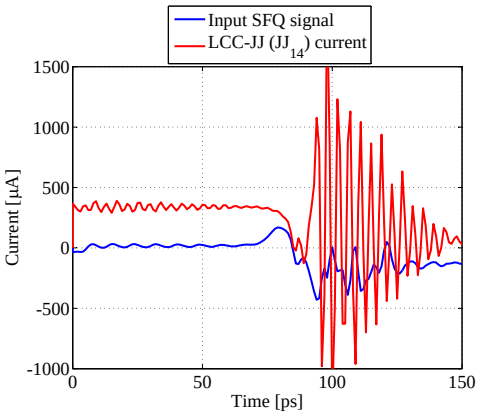
Figure 3.9 shows a graph of the current through the Suzuki stack amplifier against time. For the graph, the clock signal at V_4 is high. Figure 3.9a shows the current through the input LCC-Josephson Junction (JJ_8). As the clock is high, the initial current through the junction is 351 μA. When the SFQ signal is introduced into the Suzuki stack amplifier, the current through JJ_8 increases above its critical current (I_c = 450 μA). That switches JJ_8 to its resistive state, and all the current delivered from V_4 goes through the HCC-Josephson Junction leg of the amplifier. Figure 3.9b shows that the current through JJ_{13} drops as soon as the SFQ signal is introduced into the circuit.

Figure 3.10 shows the current through the HCC-Josephson Junction (JJ_{12}) leg of the amplifier. When all the current delivered from V_4 goes through the HCC-Josephson Junction leg of the amplifier, the current through JJ_{12} increases above its critical current (I_c = 1 mA). That forces the junction to switch to its resistive state, and the current delivered by V_4 goes into the load resistance (R_{12}).

When JJ_{12} is switched to its resistive state, the output voltage will be the



(a) Input SFQ signal and current through the Input LCC-Josephson Junction (JJ_8) against time graph.



(b) Input SFQ signal and current through the LCC-Josephson Junction (JJ_{13} to JJ_{14}) against time graph.

Figure 3.9: Time analysis of the input SFQ signal and the current through the LCC-Josephson Junction leg of the amplifier.

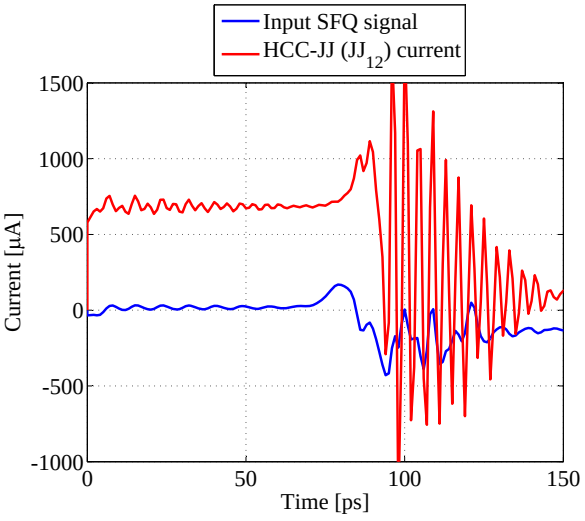


Figure 3.10: Input SFQ signal and current through the HCC-Josephson Junction (JJ_{12}) against time graph.

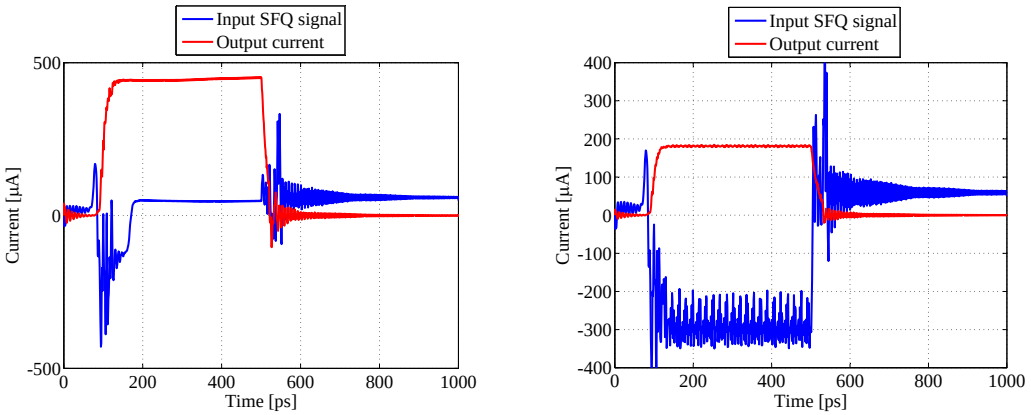
sum of the energy gaps across each Josephson Junction in the HCC-Josephson Junction leg of the amplifier. The energy caps across each Josephson Junction is just higher than 2 mV. Four HCC-Josephson Junctions in series would thus result in an output voltage of 8.1 mV.

The junctions JJ_8 and JJ_{12} will stay at their resistive states until the clock (V_4) drops to a low. That will decrease the current delivered and both junctions will return to their superconducting states. When the clock switches to high again, the delivered current will go through the Suzuki stack amplifier to ground and the output current and voltage will remain at zero until the next SFQ signal is received.

Figure 3.11 shows the input SFQ pulse and the output current of the Suzuki stack amplifier with a load resistance (R_{12}) of 18.5 Ω and 50 Ω synchronised to a 1 GHz clock signal. When the load resistance is 50 Ω or higher, some of the delivered current reflects back into the system through resistors R_{10} and R_9 to ground. The amplifier thus have a smaller output current. The input signal also takes longer to stabilise. For higher frequencies, the next high clock pulse can switch the Josephson Junction (JJ_8), because the input have not stabilised yet.

When the load resistance is too small ($R_{12} < 5.5$ Ω), some of the current delivered by V_4 goes through R_{12}. When the SFQ pulse switches the input LCC-Josephson Junction (JJ_8) to the resistive state, some of the curretn goes through R_{12} to ground. Therefore the current that goes through the HCC-Josephson Junction leg of the amplifier is not enough to switch the junction, JJ_{12} to its resistive state. The load resistance was optimised to be 18.5 Ω. For maximum current gain and bandwidth, an external matching network can be used to match the 18.5 Ω load resistance of the Suzuki amplifier with a 50 Ω transmission line.

Figure 3.12 shows the output current of the Suzuki stack amplifier against time and figure 3.13 the output voltage. A 1101 RSFQ signal was used that is synchronised to a 3.33 GHz clock signal.



(a) Input SFQ pulse and output current with a load resistance of 18.5 Ω.

(b) Input SFQ pulse and output current with a load resistance of 50 Ω.

Figure 3.11: Time analysis of the input SFQ pulse and the output current of the amplifier synchronised to a 1 GHz clock signal.

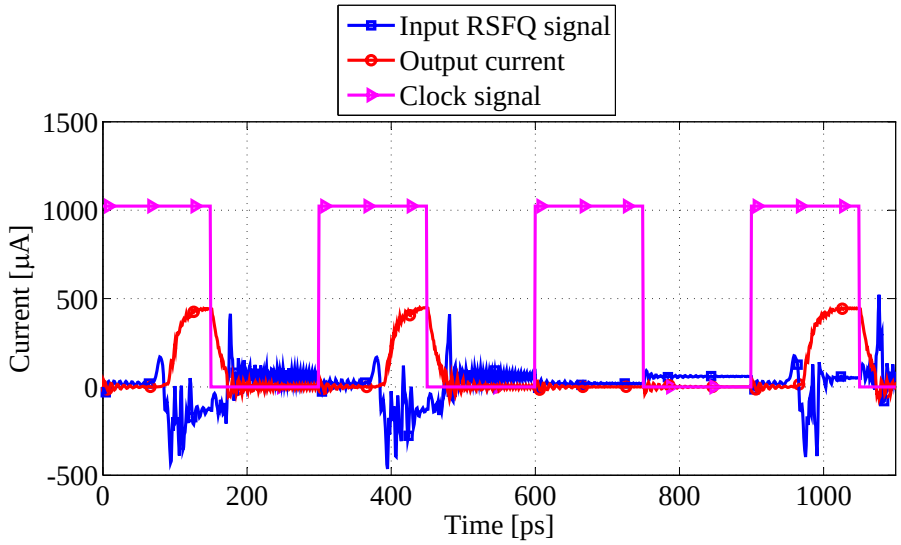


Figure 3.12: Time analysis of the output current of the Suzuki stack amplifier.

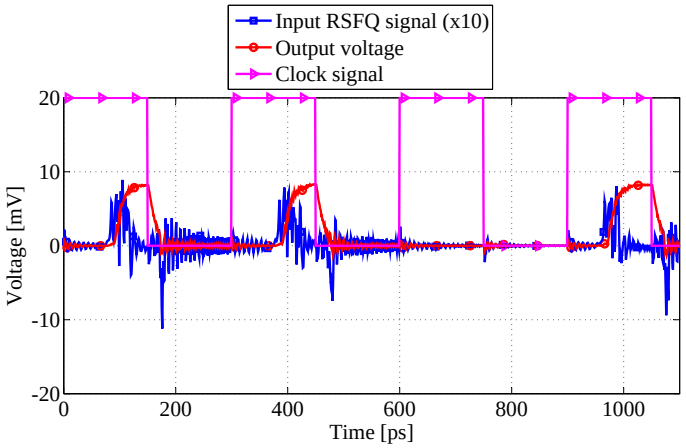


Figure 3.13: Time analysis of the output voltage of the Suzuki stack amplifier.

3.1.6 Monte Carlo Analysis

The manufacturing of a SCE circuit will always have a number of uncertainties. The manufacturing will be done using the Hypres Niobium Integrated Circuit Fabrication [21]. A global tolerance of 10% is specified for the Junction critical current density (J_c), 20% for the sheet resistance, 10% for the inductance and 5% for the junction capacitance. Local tolerances contain the more accurate models, which were derived through parameter extractions by [7] from circuit layouts. Those models incorporate the actual layout values of and local tolerances specific to each element. The local tolerances were calculated to be 5% for the J_c, 5% for the junction area, 5% for the resistance and 15% for the inductance. Table 3-I shows the global and local tolerances for the Hypres 1 kA/cm² niobium process. The local tolerance in junction capacitance does not need to be set, since it depends on the area of the junction alone.

Global tolerances result from layer thickness variations and local tolerances from element width or junction area variations. A Monte Carlo simulation file was created that model the global and local tolerances. Each component value was multiplied by a Gaussian distributed random value of both the component's global and local tolerance.

The Monte Carlo simulation measured the output of the complete SCE with

Table 3-I: Global and local tolerances for Hypres 1 kA/cm^2 niobium process.

Parameter	**Global tolerance**	**Local tolerance**
J_c	10 %	5 %
Junction area	-	5 %
Resistance	20 %	5 %
Inductance	10 %	15 %
Junction capacitance	5 %	-

a digital 1101 3.33 GHz RSFQ input. Figure 3.13 shows the desired output voltage of the SCE. The Monte Carlo simulation measured the output voltage from 5 ps to 20 ps, 300 ps to 350 ps, 600 ps to 750 ps and 900 ps to 940 ps. The average voltage must be below 1 mV in those time intervals to make sure the clock signal did not switch the junctions of the Suzuki stack amplifier to their resistive state. The output voltage from 130 ps to 150 ps, 440 ps to 450 ps and 1000 ps to 1050 ps are also measured. The average output voltage must be above 5 mV in those time intervals to make sure that the amplifier detected the different SFQ signals. Table 3-II shows the measurement specifications for the SCE output voltages used in the Monte Carlo analysis.

Table 3-II: Monte Carlo measurement specifications for the SCE output voltages

Time	**Output voltage**
5 ps to 20 ps	< 1 mV
130 ps to 150 ps	> 5 mV
300 ps to 350 ps	< 1 mV
440 ps to 450 ps	> 5 mV
600 ps to 750 ps	< 1 mV
900 ps to 940 ps	< 1 mV
1000 ps to 1050 ps	> 5 mV

The Monte Carlo analysis was run 441 times on the complete SCE circuit with different Gaussian tolerance values for each component. The output was measured with the above mentioned specifications and the circuit was either flagged as 'fail' or 'pass'. Figure 3.14 shows the results from the Monte Carlo analysis.

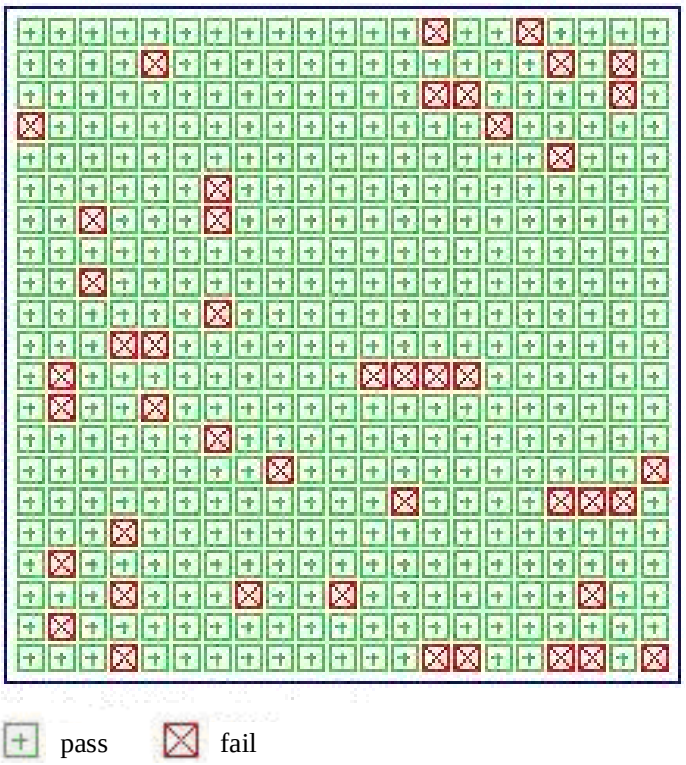


Figure 3.14: Results from the Monte Carlo analysis done on the complete SCE circuit.

The uncertainty interval is calculated for a confidence level of 99 % [25]. If the observed yield for N Monte Carlo cycles is y', then the uncertainty interval is given by

$$L = 2.6\sqrt{\frac{y'(1-y')}{N}}, \tag{3.3}$$

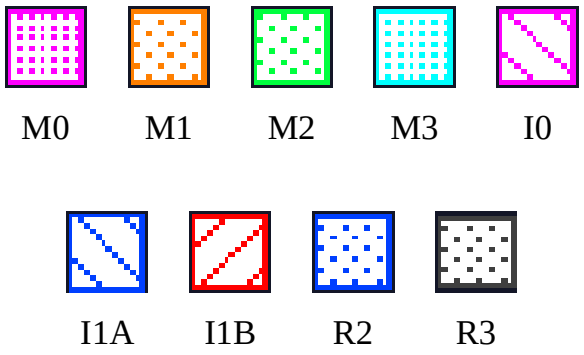
and the statistical yield y is

$$y = y' \pm L. \tag{3.4}$$

The Monte Carlo analysis predicts a yield of 89.9 %. From equation 3.3 and equation 3.4 the Monte Carlo analysis predicts a uncertainty interval of 3.7 % and a statistical yield of 89.9 ± 3.7 %. However, the success of the circuit is mainly related to the current received from the clock signal. Either the initial current through the LCC-JJ leg of the Suzuki amplifier was too high and the circuit amplified the clock signal, or it was too low and the circuit couldn't detect the SFQ signal. The current through the Suzuki stack amplifier is controlled through an external source and can be adjusted until the correct output is received. This enables circuits that fail with normal inputs to be tuned during testing and improve the success rate.

3.1.7 SCE Layout

The layout of the circuit was done with Lasi 6. The Hypres process #03-10-45 design rules were used [21]. Square area Josephson Junctions were used and the connections between the components were kept as small as possible. The inductances between the connections were calculated with the sline.exe program [26]. The layout key is shown in figure 3.15 [21]. Figure 3.16 shows the Lasi 6 layout of the DC-to-SFQ converter, figure 3.17 the 250 μA JTL and figure 3.18 the Suzuki stack amplifier. The JTL250 and the DC-to-SFQ cells were created by [7]. Figure 3.19 shows the complete layout of the SCE in Lasi 6. Figure 3.2 on page 31 shows the circuit schematic in WRSpice.



Layer	Material
M0	Nb
M1	Nb
M2	Nb
M3	Nb
I0	SiO_2
I1A	AlO_x
I1B	Contact
R2	SiO_2
R3	Au

Figure 3.15: Layer key for the layout mask.

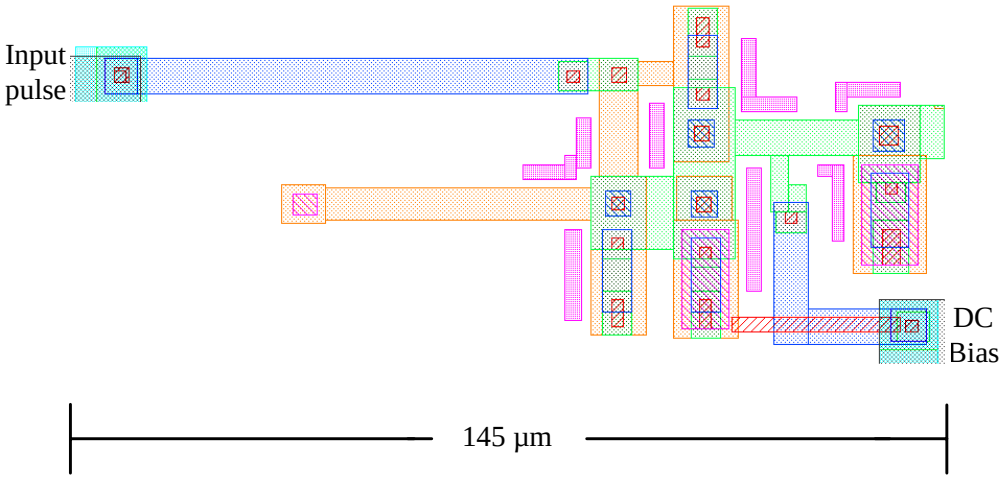


Figure 3.16: Layout of the DC-to-SFQ.

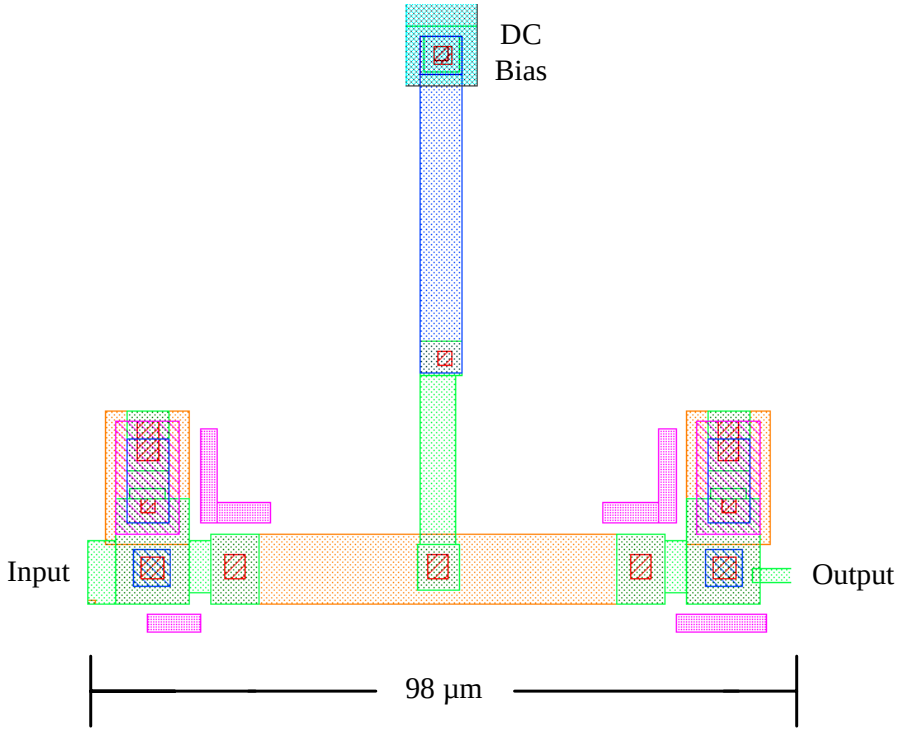


Figure 3.17: Layout of the 250 μA JTL.

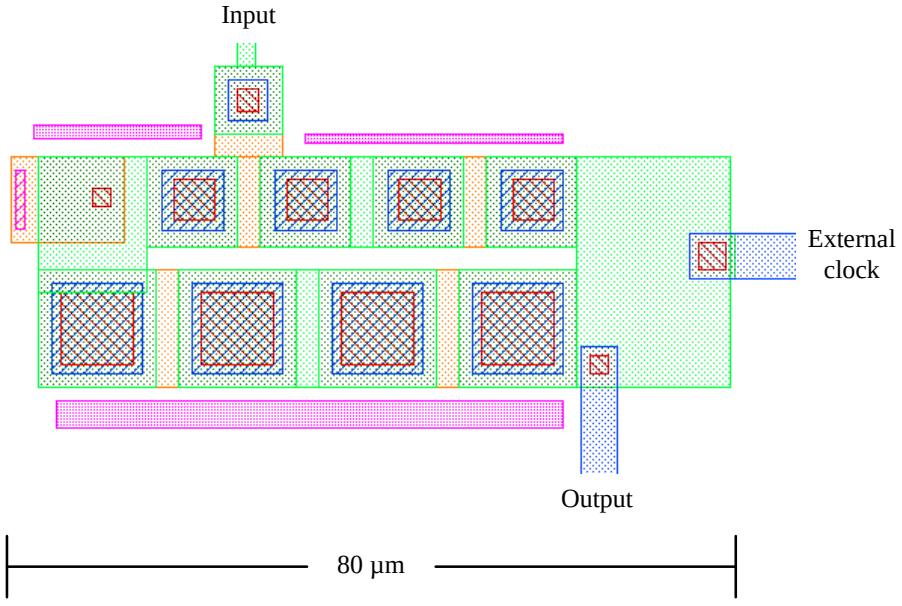


Figure 3.18: Layout of the Suzuki stack amplifier.

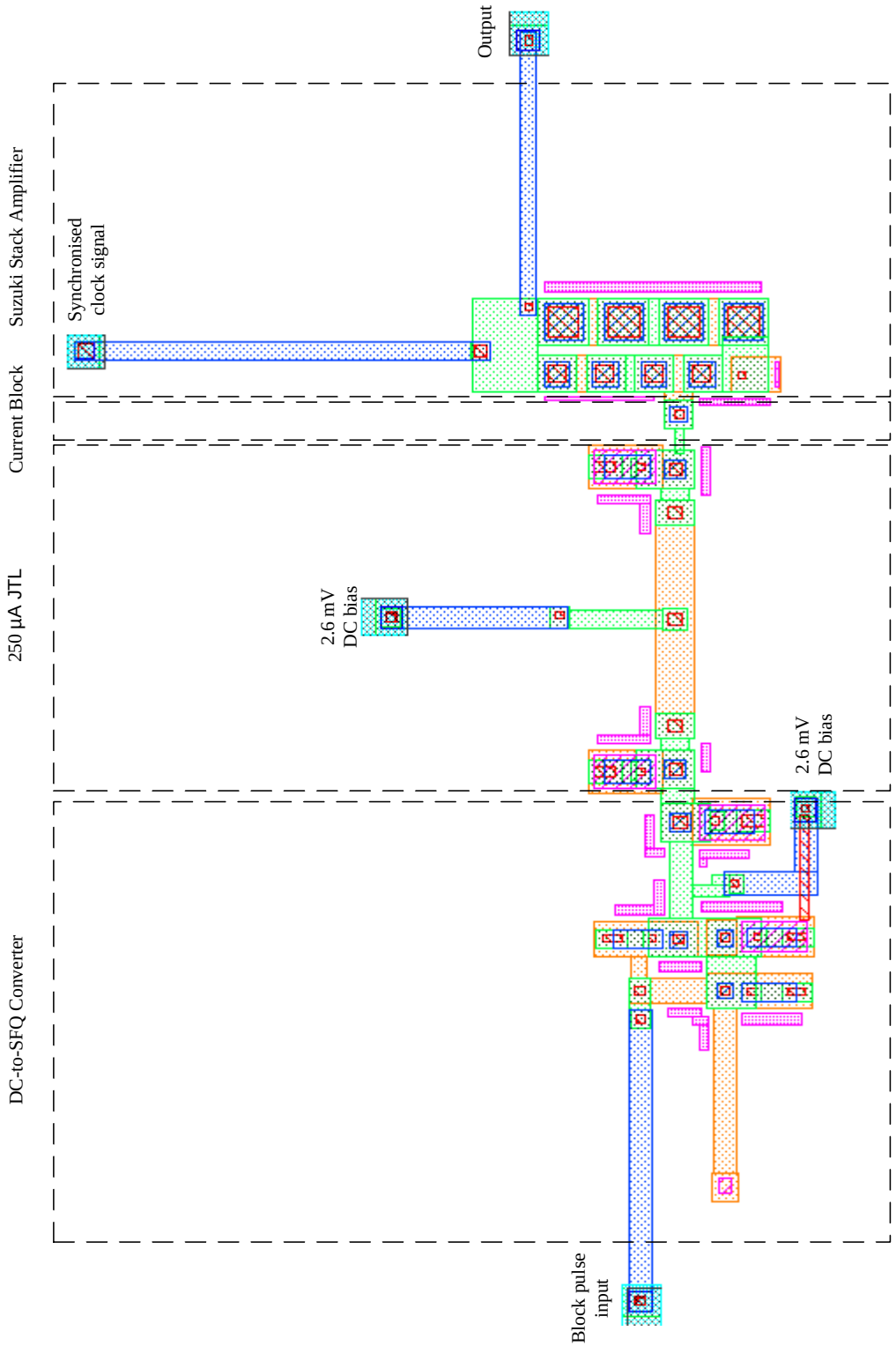


Figure 3.19: Complete layout of the SCE.

3.2 Cryogenic Measurements Block Diagram

A block diagram of the cryogenic measurements of the commercially available CMOS amplifier IC's is presented in figure 3.20.

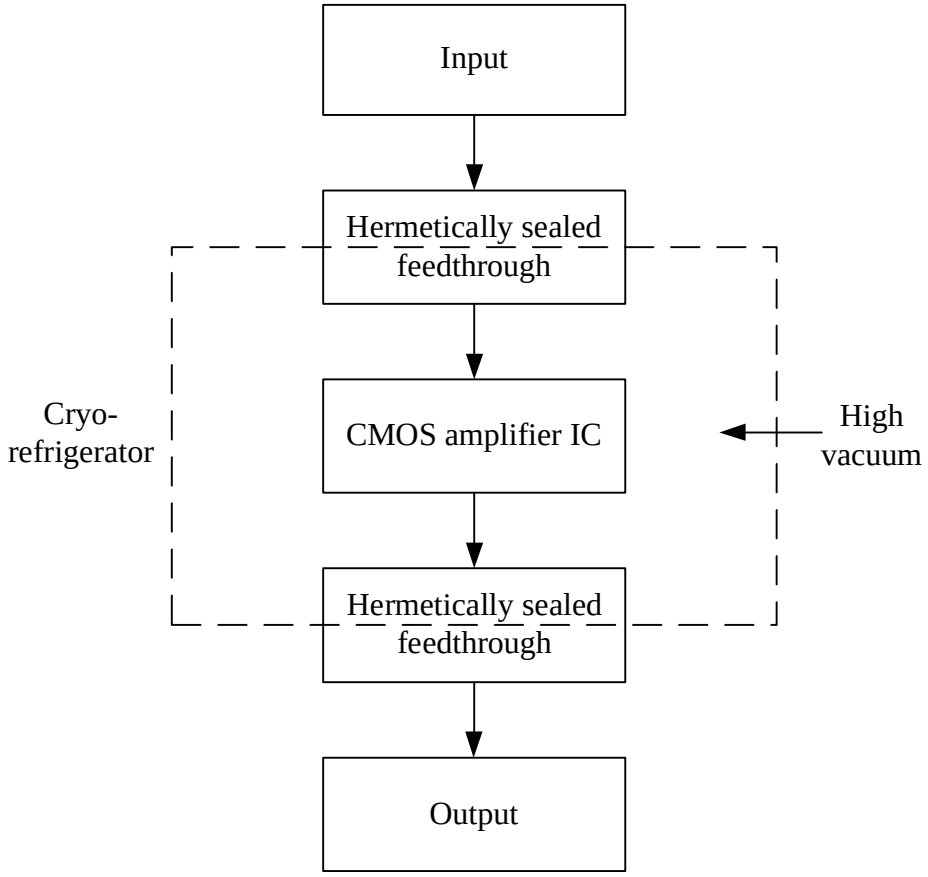


Figure 3.20: Block diagram of the experimental setup of the CMOS amplifiers.

The amplifier circuitry is soldered onto a specifically designed Printed Circuit Board (PCB). The PCB is connected directly onto the cold finger of the cryorefrigerator and covered with a solid brass cover. That will insure that the amplifier IC reaches the same temperature as the cold finger.

Signals are fed in and out of the cryorefrigerator through two hermetically sealed SubMiniature version A (SMA) connectors. The connectors would

allow access into the cryorefrigerator without breaking the vacuum required within the cryorefrigerator. The measurement equipment are at room temperature while the amplifier IC is cooled down to 4 K.

3.2.1 Cryogenic Measurements Setup

Ten commercially available CMOS amplifier IC's was selected and tested in the Cryorefrigerator. The PCB is designed to be $25.4mm \times 25.4mm$. As explained in section 2.9, SMD film resistors are used. The resistors has a uniform 30 % increase in resistivity at 4.2 K [8], but the smaller SMD package types are required to fit all the components on the PCB. The resistors can be designed to have the desired resistivity at 4.2 K.

Tantulum SMD capacitors were used when capacitances larger than 0.1 μF was required, and Polystyrene Axial capacitors for smaller capacitances. From section 2.9, one can see that the Tantalum SMD capacitors have a less than 20 % decrease in capacitance at 4.2 K, while the Polystyrene Axial capacitors have a 10 % increase at the same temperatures. The capacitors are mainly used as DC-blocking and bypass capacitors, and a 20 % difference in capacitance is acceptable.

The PCB's were designed in Protel DXP and manufactured with FR4 PCB material. The tracks are covered with a Tin (Sn) layer. The back plane of the PCB is covered with the Sn layer, that acts as a solid ground layer. Each individual amplifier circuit is placed in the centre of the PCB and surrounded with a Sn layer that also acts as a ground.

A solid brass cover was designed and is illustrated in figure 3.21. The cover has a width of 25 mm and a length of 35 mm. There is a square hole inside the cover with a length and width of 22 mm and a depth of 10 mm. The front of the hole is covered with two 23_SMA-50-0-1/111_NE female panel connectors from Huber and Suhner. The PCB is screwed against the cold finger of the cryorefrigerator with the brass cover. The amplifier components fit inside the hole of the brass cover and the input and output of the amplifier

is connected to the SMA connectors. The PCB is slightly larger than the hole in the brass cover, which forces the brass cover to press the PCB against the cold finger of the cryorefrigerator. The cover presses against the ground edges of the PCB forcing the whole cryorefrigerator to be a ground plane. Two copper wires are connected to the V_{cc} and V_{ee} of the amplifiers and led out of the brass cover between the SMA connectors.

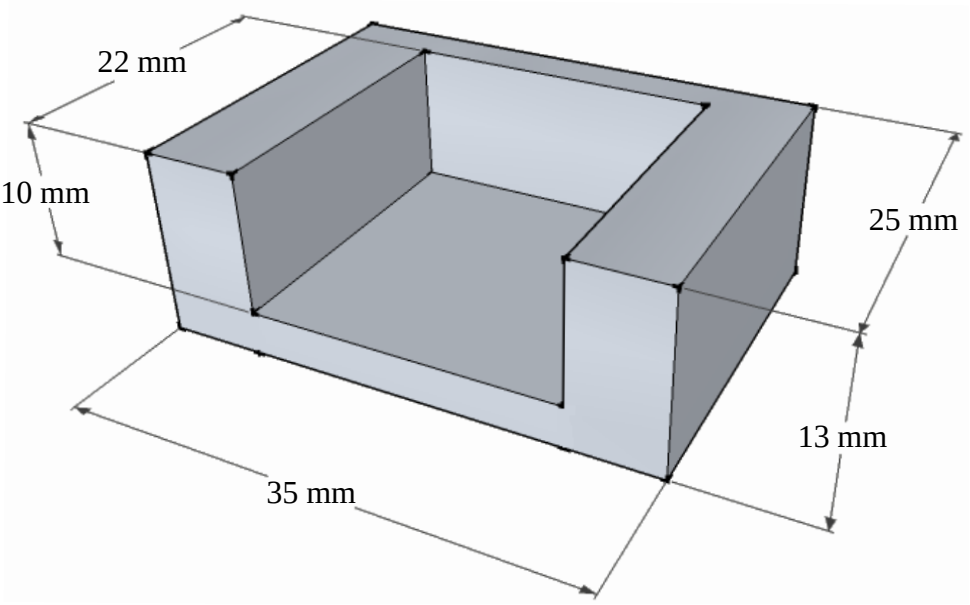


Figure 3.21: 3D illustration of the brass cover.

Figure 3.22 shows a photograph of the brass cover, the PCB and the brass plate used to screw the cover against the cold finger of the cryorefrigerator. Figure 3.23 shows the PCB connected to the cold finger.

Two hermetically sealed 34_SMA-50-0-3/111_NE female-to-female SMA feedthrough adaptors are used to feed the input and output of the amplifiers through the cryorefrigerator. The connectors have a leakage rate of 10^{-6} Torr l/sec, which is low enough to hold the vacuum inside the cryorefrigerator. 50 Ω RG 316 cable is used between the SMA connectors of the brass cover, and the SMA feedthrough's. The cable uses two male

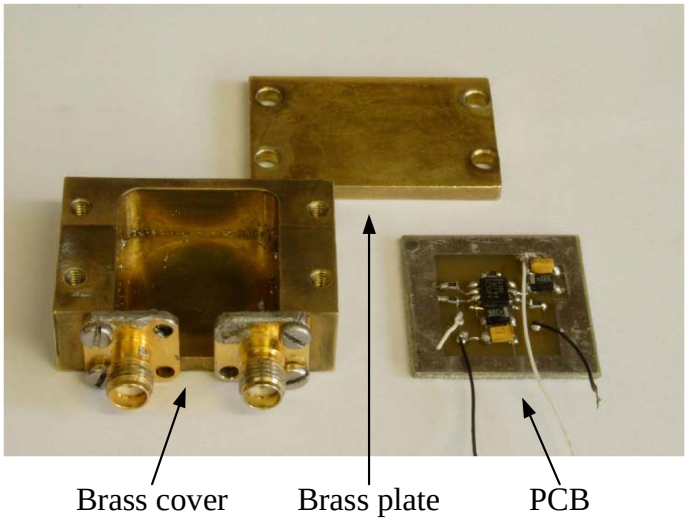


Figure 3.22: Photograph of the brass cover, the PCB and the brass plate used to connect the PCB to the cold finger.

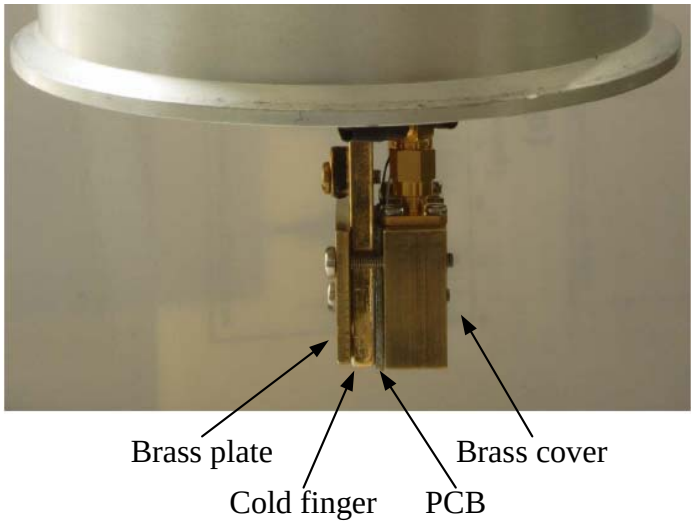


Figure 3.23: Photograph of the PCB connected to the cold finger of the cryorefrigerator.

11_SMA-50-1-4/111_N cable connectors. The datsheet of the cable shows a maximum operating frequency of 3 GHz [27]. The cable was thermal grounded to the first and second stages of the cryorefrigerator to reduce the heat transfer. The cryorefrigerator is able to reach 2.6 K on the cold finger without the cable and 4 K with the cable inside the cryorefrigerator. The same cable and connectors are used outside the cryorefrigerator.

Figure 3.24 shows a photograph of the measurement equipment used in the experiments and figure 3.25 shows a photograph of the cryorefrigerator. The scattering-parameters of the amplifier were measured outside the cryorefrigerator with the *Rohde and Schwartz FSH-Z3* handheld Spectrum Analyser connected to its VSWR bridge. The noise figure was measured with the *HP 8970B* Noise Figure Meter connected to an external noise source and the temperature inside the cryorefrigerator was measured with the *9700 Temperature Controller* from Scientific Instruments.

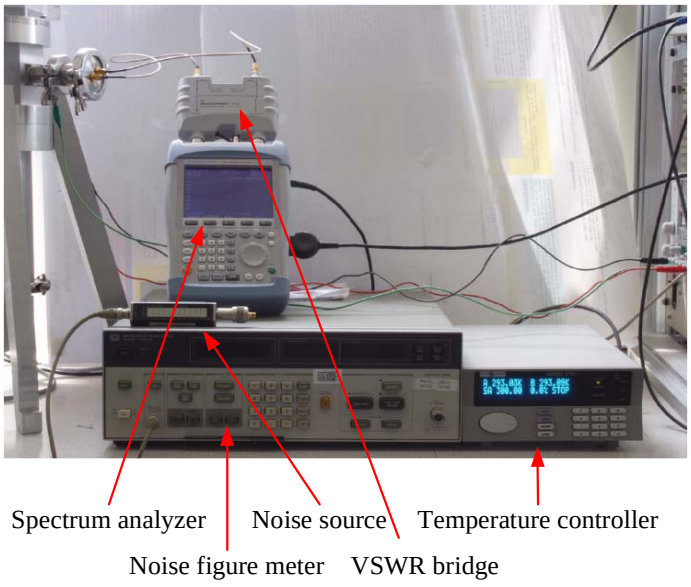


Figure 3.24: Photograph of the measurement equipment used in the experiments.

Figure 3.25: Photograph of the cryorefrigerator.

Chapter 4

Measurements and Results

In order to verify the theoretical design of the previous chapters, practical experimentation was performed. This chapter describes the conditions under which each experiment were performed and provide the results. A brief interpretation of each result is included.

4.1 Suzuki Stack Amplifier

The complete theoretical design of the Suzuki stack amplifier and all the sub-circuits required is explained in section 3.1. The amplifier was simulated in WRSpice. The amplifier is synchronised with an external clock signal. The clock signal can have any frequency between DC and 7 GHz and an amplitude between 19.7 mV and 20.3 mV when it is high. The amplifier must receive the SFQ signal while the clock is high.

The 250 μA JTL delays the SFQ signal by 16 ps and the current block delays it by a further 4 ps. The Suzuki stack amplifier has a rise time of 33 ps and a fall time of 31 ps. That gives a total delay of 53 ps for the Suzuki stack amplifier to reach its maximum value after the SFQ signal has been introduced. As explained in section 3.1.5., the output would stay high as long as the clock is high. That means that the lower the synchronised clock frequency, the wider the width of the output signal in the time domain and the easier the synchronisation.

The gain of the amplifier can be determend from figures 3.12 and 3.13 on pages 41 and 42. The output voltage in the presence of a 600 μV SFQ pulse is 8.2 mV. The output current in the presence of a 160 μA SFQ pulse is 430 μA.

The biggest advantage however, is in the time spread of the signal. The output signal remains high until the clock undergoes a high-to-low transmission, effectively slowing down the signal. It is thus detectable by lower frequency circuitry.

4.2 Commercially Available Amplifiers

Commercially available CMOS amplifiers were tested. Ten different amplifier ICs were ordered from Maxim Integrated Products Inc., Texas Instruments Inc. and Hittite Microwave Corp.

The Max4304, Max4305, Max2659 and Max2644 amplifiers were ordered from Maxim Integrated Products Inc. Unfortunately Maxim would not divulge information on the manufacturing process of their amplifiers. However, power consumption and gain bandwidth improves through decreasing channel length in MOS devices [28]. These four different amplifiers were chosen because they have high bandwidth, low noise figure and low supply current.

The THS4503, THS3201, THS4304 and THS3062 amplifiers were ordered from Texas Instruments Inc. THS3201 and THS4503 are wideband high-speed amplifiers with a low noise figure and supply current. THS3062 is a current feedback amplifier utilising the Texas Instruments BiCom-I process, while THS4304 is a voltage feedback amplifier utilising the Texas Instruments BiCom-III process.

The Texas instruments BiCom-III process is designed for exceptionally high-frequency operation in signal conditioning and data conversion [29]. Using the high-speed of the 0.35 μm CMOS process, the BiCom transistors are designed with the best high performance component set. It achieves exceptionally

high-frequency operation in signal conditioning and data conversion.

The HMC548 and HMC460 amplifiers were ordered from Hittite Microwave Corp. The HMC548 comprises two internally matched SiGe Heterojunction Bipolar Transistor (HBT) Low Noise Amplifier (LNA) stages which operate from 1.2 GHz up to 3 Ghz [30]. The HMC460 is a GaAs p-HEMT low noise distributed amplifier which can operate from DC to 20 GHz [3].

These ten amplifiers were placed inside the cryocooler to test their functionality in low temperatures. Table 4-I shows the summarised results of the ten amplifiers tested in cryogenic environments. The Gain-bandwidth product in the table is the bandwidth given in the data sheets for a minimum gain of $A_v = 5$. The indicated failure temperature was measured where the *Tektronics* digital oscilloscope could not detect the output signal. The minimum temperature achieved in the cryorefrigerator was 4 K.

Table 4-I: Lower temperature limit of tested amplifiers.

Amplifier	**Type**	**Gain-bandwidth [MHz]**	**Failure temperature [K]**
MAX4304	CMOS	DC to 540	90
MAX4305	CMOS	DC to 340	85
MAX2659	SiGe BiCMOS	1250 to 2250	70
MAX2644	SiGe BiCMOS	2400 to 2500	80
THS4503	BiCOM-I	DC to 300	90
THS3201	BiCOM-I	DC to 500	95
THS4304	BiCom-III	DC to 870	-
THS3062	BiCom-I	DC to 100	109
HMC548	SiGe HBT	900 to 3 000	-
HMC460	p-HEMT	DC to 10 000	-

From table 4-I it can be seen that there were three amplifiers that remained functional at temperatures as low as 4 K. Each amplifier that did not work down to 4 K and the HMC548 amplifier, was only tested once. It was assumed that all identical amplifier IC's will have the same results when cooled down.

However, five different THS4304 IC's and three different HMC460 IC's were tested. Each test gave the same results, confirming the assumption.

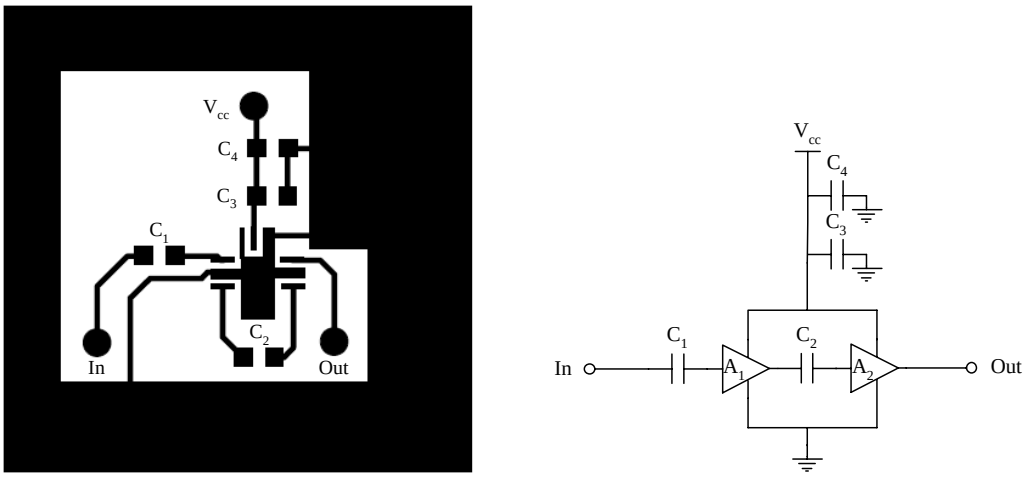
4.2.1 HMC548 SiGe HBT Amplifier

The HMC548 comprises two internally matched SiGe HBT Monolithic Microwave Integrated Circuit (MMIC) low noise amplifier stages with a bandpass filter between the two stages [30]. The bandpass filter allows the receiver to reject nearby blocking signals, without incurring the noise figure degradation associated with a high rejection pre-filter. The LNA is mainly used as a receiver pre-amplifier. Its datasheet shows a bandwidth from 900 MHz to 3 GHz with a maximum gain of 20 dB at 1.3 GHz.

Figure 4.1 shows the PCB and the schematic layout of the HMC548 amplifier. The HMC548 is powered by a single supply voltage $V_{cc} = +5V$. The circuit was built on an FR4 PCB. The bandpass filter was replaced by a single 150 pF capacitor (C_2). C_1 acts as a off chip DC blocking capacitor and C_3 and C_4 as bypass capacitors. Polystyrene axial capacitors were used for all the capacitors. Table 4-II shows the values of the components used in the HMC548 amplifier.

Table 4-II: Component values for the HMC548 amplifier

Component	**Value**
C_1	150 pF
C_2	150 pF
C_3	1.2 nF
C_4	68 nF
A_1	On chip LNA
A_2	On chip LNA
V_{cc}	+5 V



(a) PCB layout of the HMC548 amplifier.

(b) Schematic layout of the HMC548 amplifier.

Figure 4.1: PCB and schematic layout of the HMC548 amplifier.

The frequency response of the amplifier was measured at room temperature (300 K) and then again at 4 K. From the graph in figure 4.2 one can see the temperature variations decreased the gain of the amplifier with a maximum of 4 dB. The amplifier still showed a maximum gain of 20 dB at 4 K.

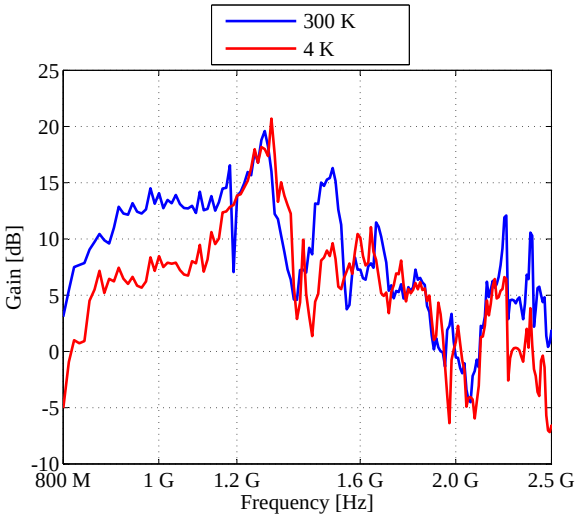


Figure 4.2: Frequency response of the HMC548 amplifier at 300 K and 4 K

4.2.2 HMC460 GaAs p-HEMT Low Noise Amplifier

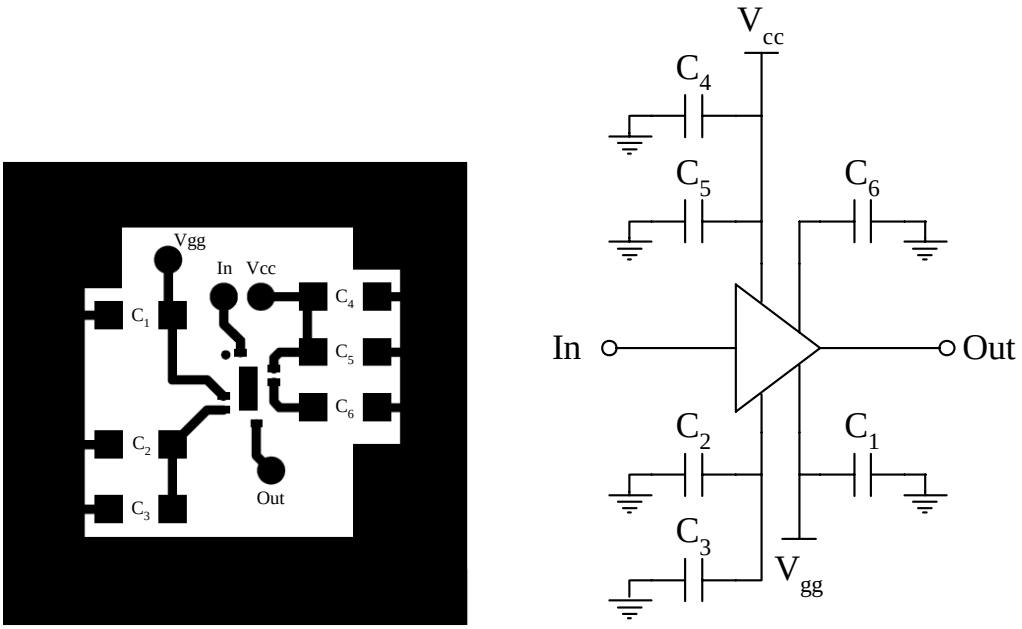
The HMC460 is a GaAs MMIC p-HEMT low noise amplifier from Hittite Microwave Corp. According to its datasheet [3], it has a gain of 14 dB from DC to 10 GHz with a noise figure as low as 3.5 dB. The gain flatness is ± 0.5 dB but, it requires 75 mA from a DC power supply.

Figure 4.3 shows the PCB and schematic layout of the HMC460 amplifier. The amplifier was received as a die without a package. The die was attached directly to the ground plane of an FR4 PCB. Microstrip transmission lines were then wirebonded to the die. The input and output of the PCB were connected to the SMA connectors of the brass cover in section 3.2.1. V_{gg} was adjusted to achieve I_{cc} = 75 mA. C_4 and C_6 are tantalum SMD capacitors while C_1, C_2, C_3 and C_5 are polystyrene axial capacitors.

Table 4-III shows the values of the components used in the HMC460 amplifier.

Table 4-III: Component values for the HMC460 amplifier

Component	**Value**
C_1	1.2 nF
C_2	100 pF
C_3	100 nF
C_4	1 μF
C_5	1.2 nF
C_6	0.1 μF
V_{cc}	+ 6.8 V
V_{gg}	- 1.3 V



(a) PCB layout of the HMC460 amplifier.

(b) Schematic layout of the HMC460 amplifier.

Figure 4.3: PCB and schematic layout of the HMC460 amplifier.

The scattering-parameters (s-parameters) of the amplifier were measured at 300 K and then again at 4 K. Figure 4.4 shows a graph of the gain (S_{21}-parameter) of the HMC460 amplifier.

From the graph one can see that the decrease in temperature results in a 2 dB decrease in gain. The amplifier has a much flatter gain spectrum than the HMC548 and stretched from DC to 1 GHz with a maximum gain of 15.6 dB at 4 K. The amplifier had a much lower bandwidth than specified in the datasheet, because optimum RF components were not used in the layout.

Figure 4.5 shows the voltage reflection coefficient at the input port (S_{11}) and figure 4.6 at the output port (S_{22}) of the amplifier. The reflection coefficients were measured at 300 K and then again at 4 K.

From the above mentioned graphs, one can see that the amplifier is relatively well matched (< -15 dB) at lower frequencies ($f < 200$ MHz). The matching

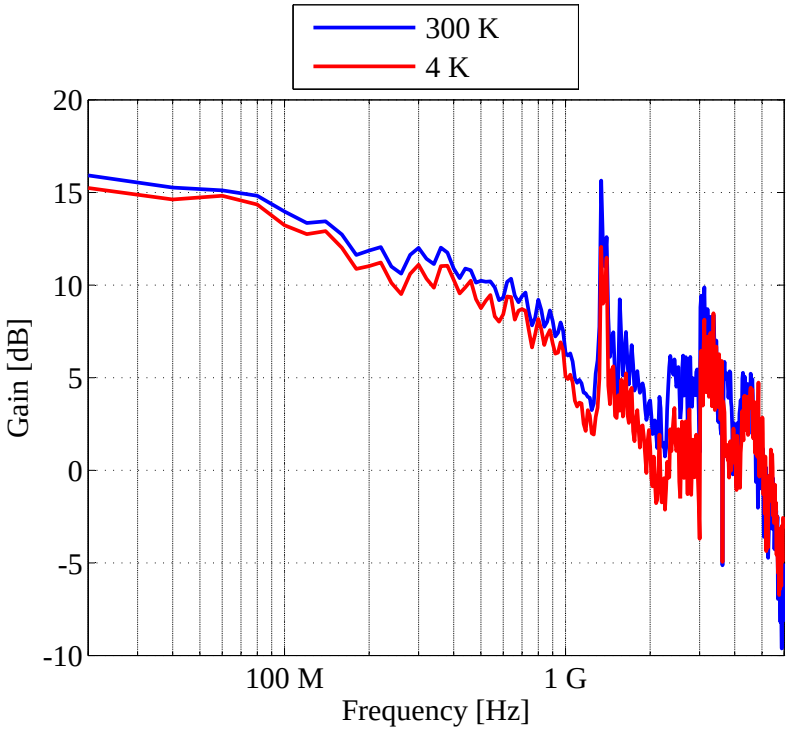
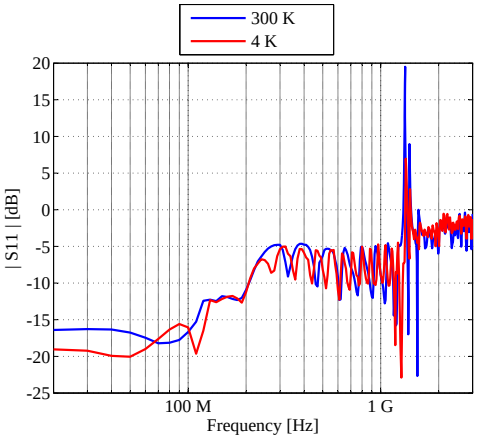
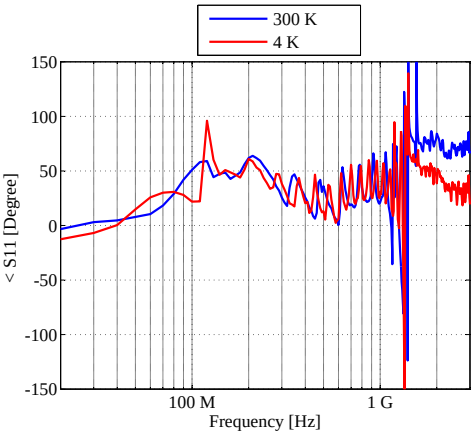


Figure 4.4: Frequency response of the HMC460 amplifier at 300 K and 4 K

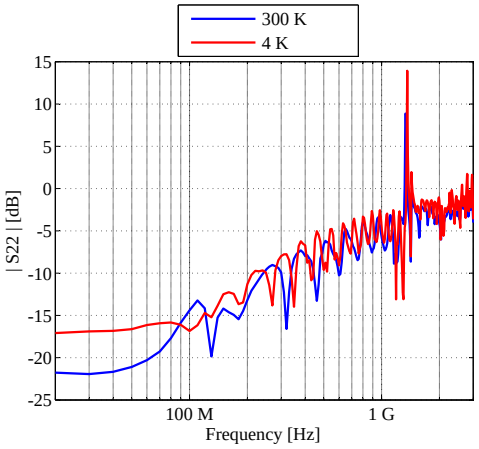


(a) Magnitude of the S_{11}-parameter for the HMC460 LNA at 300 K and 4 K.

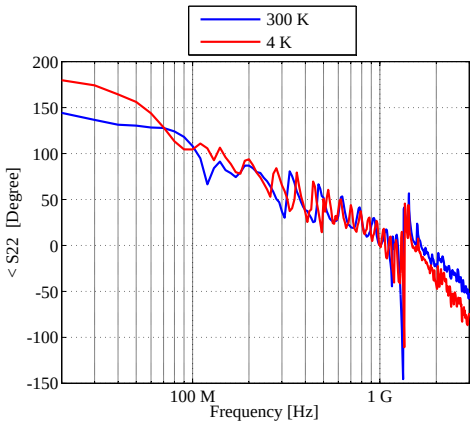


(b) Phase of the S_{11}-parameter for the HMC460 LNA at 300 K and 4 K.

Figure 4.5: Input voltage reflection coefficient (S_{11}-parameter) of the HMC460 LNA.



(a) Magnitude of the S_{22}-parameter for the HMC460 LNA at 300 K and 4 K.



(b) Phase of the S_{22}-parameter for the HMC460 LNA at 300 K and 4 K.

Figure 4.6: Output voltage reflection coefficient (S_{22}-parameter) of the HMC460 LNA.

deteriorates at higher frequencies. That is because the PCB, the connections, the components, the SMA connectors and even the cables are not optimised for high frequencies. When the amplifier is cooled down, one can see a 3 dB decrease in $|S_{11}|$ at lower frequencies which indicates a better input matching. There is a 4 dB increase in $|S_{22}|$ at lower temperatures, which indicates a slightly worse output matching. The change in the reflection coefficients at cryogenic temperatures are small enough to be neglected for the HMC460 LNA.

The quiescent power (P_Q) of the amplifier is the power consumed by the amplifier with no input. P_Q is given by

$$P_Q = V_{cc} \times I_{cc} + V_{ee} \times I_{ee}, \tag{4.1}$$

with the input signal grounded.

The quiescent power of the HMC460 LNA is calculated as 281 mW at 300 K. When the amplifier is cooled down to 4 K, the quiescent power increases to 292 mW. The cryorefrigerator can cool the IC to 6.5 K when the amplifier is switched on. To achieve measurements at 4 K, the amplifier must be switched off for an extended period and switched on briefly after the cryorefrigerator

reaches 4 K.

The noise figure of the amplifier was measured using the *HP 8970B Noise Figure Meter*. The noise figure of a network is defined to be the ratio of the signal-to-noise (S/N) power ratio at the input to the signal-to-noise power ratio at the output [31].

$$F = \frac{S_i/N_i}{S_o/N_o}. \tag{4.2}$$

From equation 4.2, the noise figure of a network is the decrease in the S/N ratio as the signal goes through the network. A perfect amplifier would amplify the noise at its input along with the signal, maintaining the same S/N ratio at its output. That will give a noise figure of 0 dB. A realistic amplifier, however also adds some extra noise from its own components and decrease the S/N ratio.

S_o and N_o represent the signal and noise levels at the output port of the amplifier. If one take N_a as the noise added by the DUT, and G as the gain of the DUT, equation 4.2 can be rewritten as

$$F = \frac{S_i/N_i}{GS_i/(N_a + GN_i)} = \frac{N_a + GN_i}{GN_i}. \tag{4.3}$$

The input noise level is usually thermal noise from the source and is referred to by kT_0B, where k is Boltzmann's constant, T_0 is the reference source temperature ($T_0 = 290K$) and B is the bandwidth of the DUT. That changes equation 4.3 to

$$F = \frac{N_a + kT_0BG}{kT_0BG}. \tag{4.4}$$

Noise figure is independent of bandwidth as long as the measurement bandwidth is narrow enough to resolve variations with frequency, because the bandwidth in the numerator cancels with the bandwidth in the denominator.

From figure 4.7, one can see that the noise figure of the HMC460 LNA dropped with more than 2 dB (to a minimum of 4.1 dB) when the amplifier

is cooled down to 4 K.

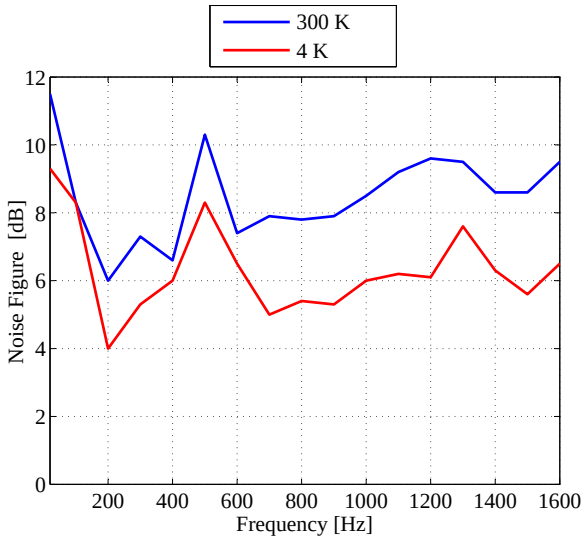


Figure 4.7: Noise figure of the HMC460 LNA at 300 K and at 4 K

An evaluation PCB was ordered from Hittite Microwave Corp. for the HMC460 amplifier. The PCB uses optimised RF circuit design techniques. The signal lines have 50 Ω impedance while the package ground leads and package bottom is connected directly to the ground plane. A sufficient number of via holes is used to connect the top and bottom ground planes.

Figure 4.8 shows the PCB layout of the Hittite Microwave Corp. evaluation board. The same capacitor values was used as in the previous PCB layout. A full list of the components can be found in table 4-III. Capacitor C_6 is a Tantalum SMD capacitor, while the remaining capacitors are Ceramic SMD. From section 2.9, one can see that Ceramic SMD capacitors work down to 220 K. The capacitors were replaced with Polystyrene Axial capacitors.

The evaluation board was connected to the cold finger of the cryorefrigerator and cooled down to 4 K. Figure 4.9 shows the gain of the HMC460 amplifier at 300 K and 4 K.

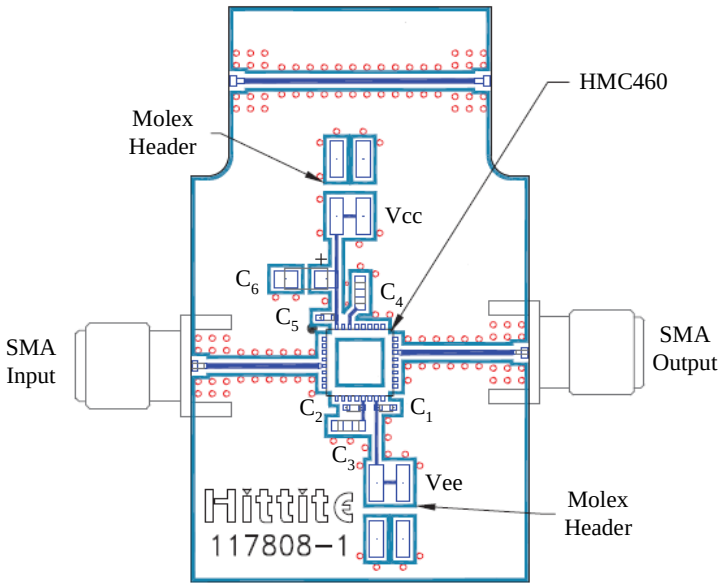


Figure 4.8: PCB layout of the HMC460 evaluation board [3].

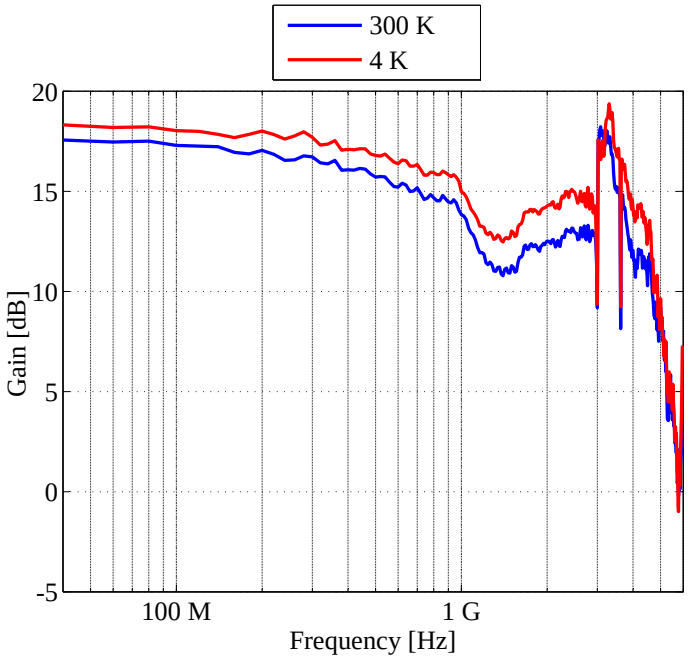
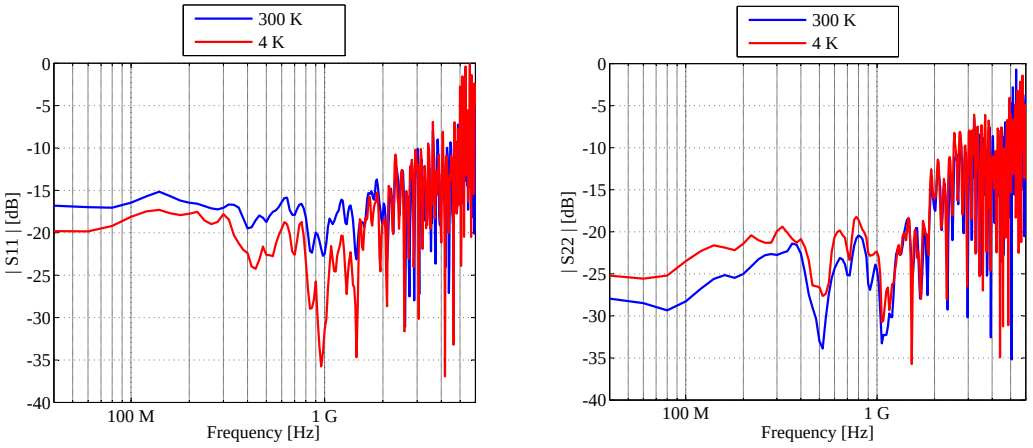


Figure 4.9: Frequency response of the HMC460 amplifier and evaluation board at 300 K and 4 K.

From the graph, one can see that the amplifier has a gain over the complete 6 GHz range of the spectrum analyser. The signal becomes distorted after 3 GHz, because the cable used inside the cryorefrigerator is only designed for signals up to 3 GHz [27]. When the amplifier is cooled down to 4 K, the gain increases with up to 1.5 dB.

Figure 4.10 shows the input and output reflection coefficient of the HMC460 amplifier build on the evaluation board. The reflection parameters were measured at 300 K and 4 K. From the graph one can see that the input reflection coefficient improved with up to 3 dB while the output reflection coefficient worsened by up to 3.5 dB. However, the output reflection coefficient remains lower than -15 dB over the band of interest.



(a) Magnitude of the S_{11}-parameters at 300 K and 4 K.

(b) Magnitude of the S_{22}-parameters at 300 K and 4 K.

Figure 4.10: Input and output voltage reflection coefficients of the HMC460 LNA build on the evaluation board.

Figure 4.11 shows the noise figure of the HMC460 LNA measured at 300 K and 4 K. From the figure one can see that the Noise Figure dropped with more than 2 dB, when the temperature was decreased to 4 K. The Noise Figure was only measured from 20 MHz up to 1600 MHz due to the limitations of the measuring equipment. The amplifier reached a minimum Noise Figure of

1.74 dB at 200 MHz with a gain of 17.4 dB.

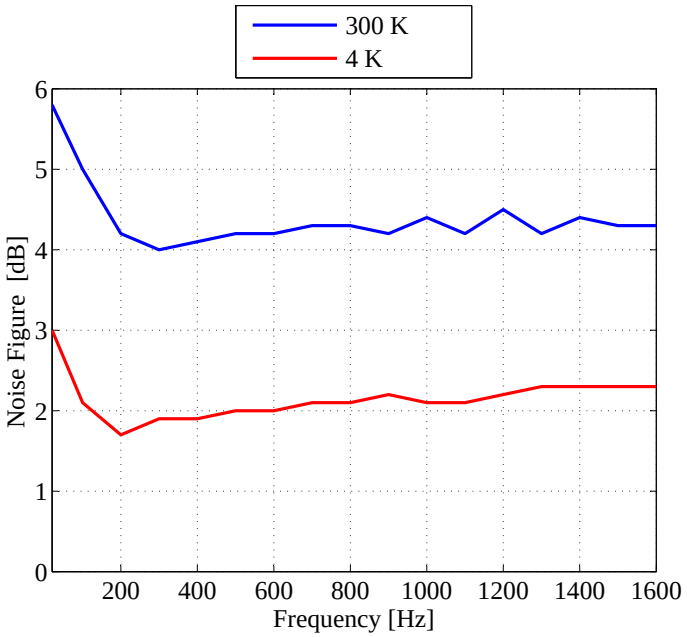


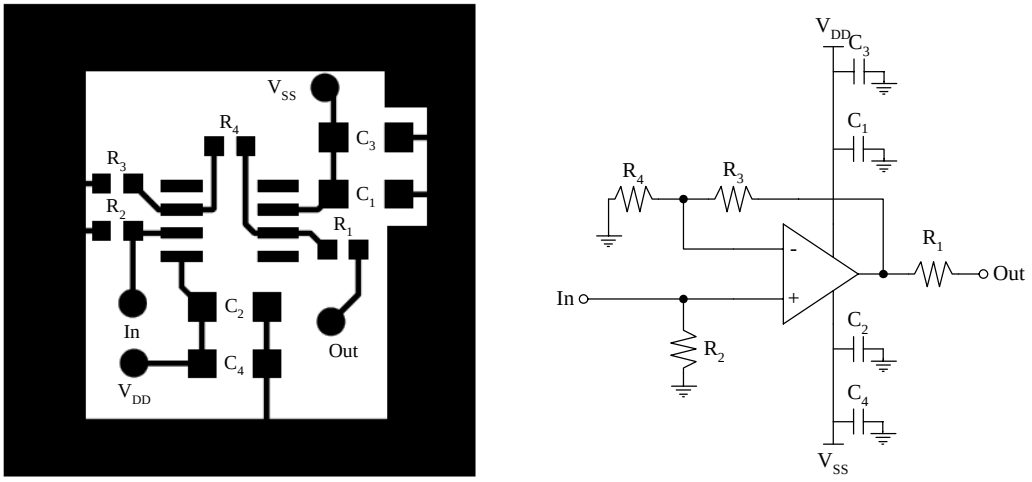
Figure 4.11: Noise figure of the HMC460 LNA at 300 K and at 4 K

4.2.3 THS4304 SiGe BiCom-III Operational Amplifier

The THS4304 is a wideband, voltage-feedback operational amplifier from Texas Instruments Inc. It was designed for high-speed, low power analog signal-processing chains and is developed in the BiCom-III SiGe process technology. It provides balanced inputs, low offset voltage and offset current, low offset drift and a high power supply rejection ratio. The process and architecture used to make the amplifier have superior noise rejection with lower power supply overhead required for proper transistor operation. The amplifier was ordered in a 8-pin Small-Outline Integrated Circuit (SOIC) package.

Figure 4.12 shows the PCB and schematic layout of the THS4304 operational amplifier. It was designed to have a non-inverting gain of 17 dB. The circuit

was soldered on a FR4 PCB. Tantalum SMD capacitors and SMD film resistors were used in the design.



(a) PCB layout of the THS4304 amplifier.

(b) Schematic layout of the THS4304 amplifier.

Figure 4.12: PCB and schematic layout of the THS4304 amplifier.

Table 4-IV shows the values of the components used in the THS4304 amplifier. C_1, C_2, C_3 and C_4 are bypass capacitors. R_1 is the output matching resistor, R_2 the input matching resistor, R_3 the feedback resistor and R_4 the gain resistor. The amplifier is powered by a dual supply voltage of $V = \pm 2.5V$.

From section 2.9, one can see that the SMD film resistors gain 30 % resistance at 4 K. The amplifier was designed to have 50 Ω input resistance and output resistance at 4 K. Consequently R_1 and R_2 was divided with 1.3. That will give a resistance value at room temperature, which will increase with 30 % at 4 K to give a matching resistance of 50 Ω.

Once again the s-parameters of the amplifier was measured at 300 K and 4 K. Figure 4.13 shows a graph of the gain of the amplifier. From the graph one can see that the amplifier worked down to 4 K. The amplifier showed an increase in bandwidth with a decrease in temperature. At 300 K the amplifier

Table 4-IV: Component values for the THS4304 amplifier

Component	**Value**
R_1	39 Ω
R_2	39 Ω
R_3	270 Ω
R_4	2.7 kΩ
C_1	0.1 μF
C_2	0.1 μF
C_3	1 μF
C_4	1 μF
V_{SS}	- 2.5 V
V_{DD}	+ 2.5 V

showed a gain of 17 dB which gradually dropped to 0 dB at 400 MHz. When cooled down to 4 K, the low frequency gain remained at 17 dB. The gain reached 0 dB only at 475 MHz. With a smaller designed gain, the bandwidth could increase up to 1.8 GHz.

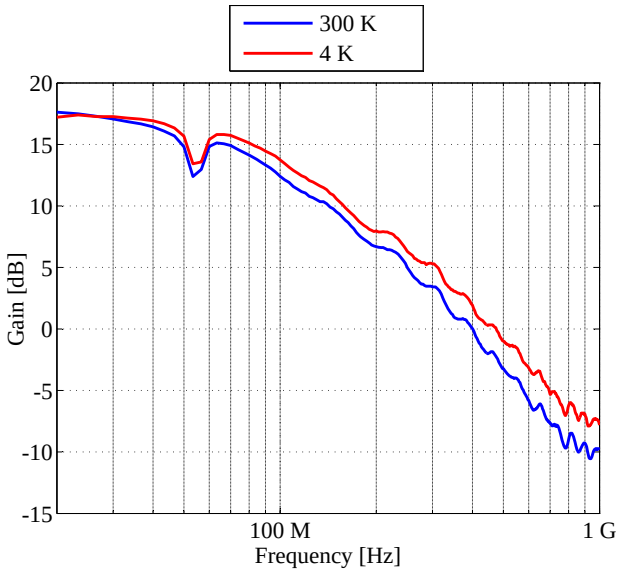
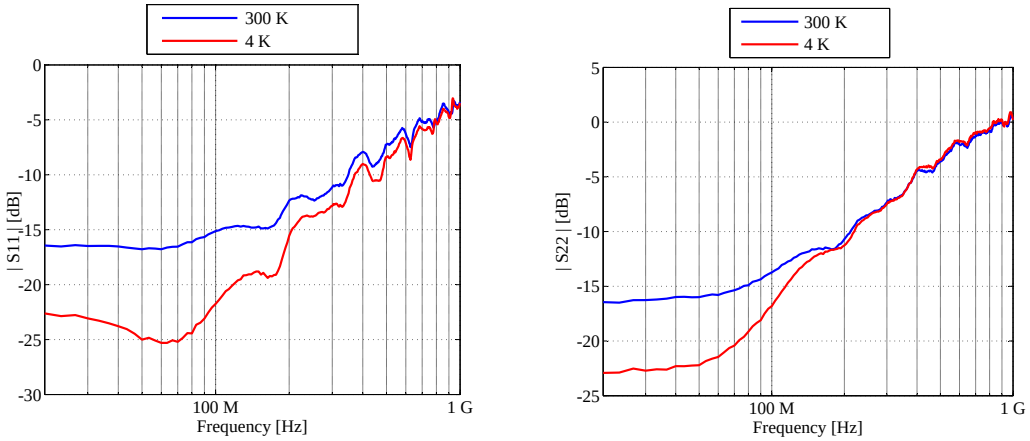


Figure 4.13: Frequency response of the THS4304 amplifier at 300 K and 4 K

Figure 4.14 shows the S_{11}-parameters and the S_{22}-parameters of the amplifier. The reflection parameters was measured at 300 K and 4 K.



(a) Magnitude of the S_{11}-parameters at 300 K and 4 K.

(b) Magnitude of the S_{22}-parameters at 300 K and 4 K.

Figure 4.14: Input and output voltage reflection coefficients of the THS4304 operational amplifier.

From the reflection coefficients, one can see that the matching of the amplifier is not optimised at 300 K. With a decrease in temperature, however, the input and load resistance increase and the reflection coefficient improves significantly.

The quiescent power of the THS4304 operational amplifier is calculated as 92 mW at 300 K. However, I_{DD} and I_{SS} decrease from 18.45 mA each down to 14.7 mA at 4 K. That gives a quiescent power of 73.5 mW, which is a 20 % decrease at 4 K.

Figure 4.15 shows the noise figure of the THS4304 amplifier measured at 300 K and 4 K. From the figure one can see that the NF dropped with more than 6 dB over the whole spectrum, when the temperature was decreased to 4 K. The amplifier reached a minimum Noise Figure of 12.8 dB at 300 MHz with a gain of 5.8 dB.

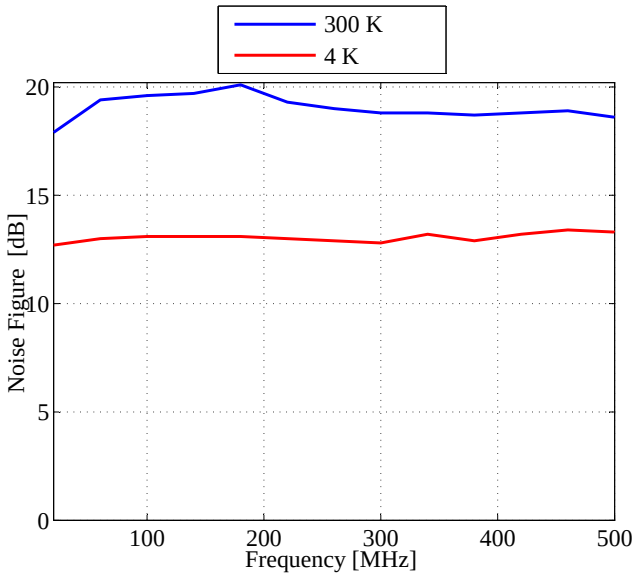


Figure 4.15: Noise figure of the THS4304 operational amplifier at 300 K and at 4 K.

4.3 Summary

Ten commercially available amplifier ICs was tested in the cryorefrigerator. Three different ICs worked at 4 K. The HMC548 amplifier has a bandwidth from 900 MHz to 3 GHz. Because it does not amplify from DC, it was not considered.

The remaining two commercial amplifiers were test further. One amplifier is a SiGe BiCom-III operation amplifier (THS4304) and the other is a p-HEMT LNA (HMC460). The THS4304 amplifier showed a 20 % decrease in quiescent power when cooled down to 4 K, while the HMC460 amplifier's quiescent power increased with less than 4 %. The quiescent power of the THS4304 was measured as 73.5 mW and the HMC460 was measured as 292 mW at 4 K.

Figure 4.16 shows the noise figure and figure 4.17 shows the gain of the two amplifiers at 4 K. The HMC460 LNA showed a gain from DC to 6 GHz with a maximum gain of 18.5 dB. It showed a minimum noise figure of 1.74 dB at 200 MHz. The THS4304 operational amplifier showed a gain from DC to 400 MHz

with a maximum gain of 17 dB. It showed a minimum noise figure of 12.8 dB at 300 MHz. The THS4304 cost only $2.35 each while the HMC460 cost $78.27.

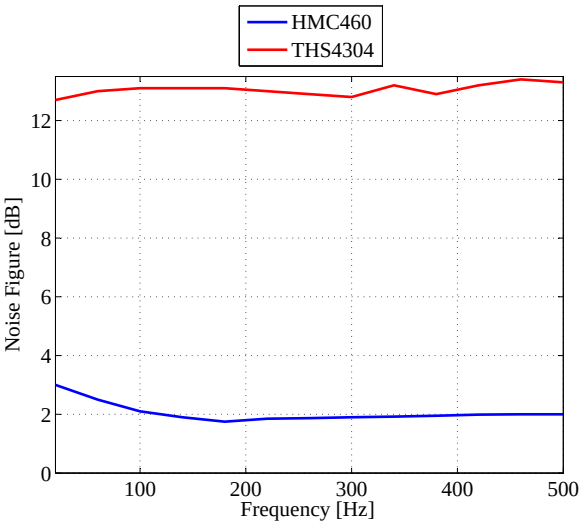


Figure 4.16: Noise figure of the HMC460 LNA and the THS4304 operational amplifier at 4 K.

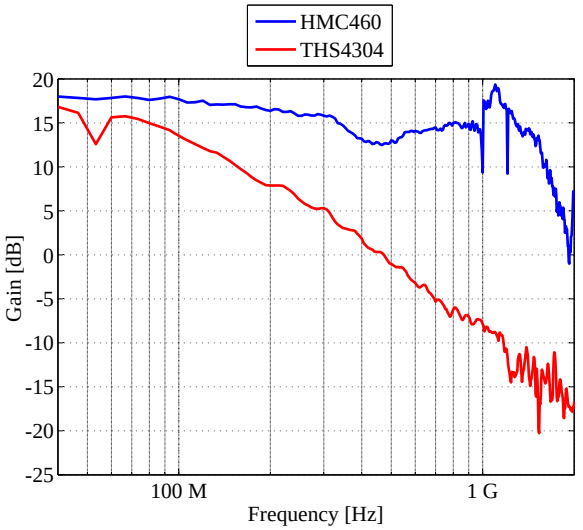


Figure 4.17: Frequency response of the HMC460 LNA and the THS4304 operational amplifier at 4 K.

Chapter 5

Conclusions and Future Work

5.1 Research Findings

The project can be divided into two main section. The first section is the SCE. The SCE was only simulated in WRSPICE and a final circuit was not developed because of cost and time restrains. The second section was the testing of commercially available amplifier ICs at 4 K. The s-parameters, noise figure and quiescent power of the amplifiers was measured and compared to its room temperature values.

5.1.1 Superconducting Electronics

Mainly two different amplifiers were considered in the SCE. The first was a DC SQUID amplifier. It consists of a single input SQUID modulating a 100-SQUID series output array through a 50-turn modulation coil. The two SQUID loops are connected in parallel, with the junction located between them. A 100-SQUID series array with an input transformer with 36 primary turns was shown by [13] to have a bandwidth of at least 175 MHz when operated alone.

The second was a Suzuki stack amplifier. The Suzuki stack amplifier is a superconducting digital logic amplifier for interfacing superconductor circuits with semiconductor circuits. It provides a gigahertz amplifier to convert low power superconducting RSFQ signals to higher power signal processing

circuits. It consists mainly of a lower I_C Josephson Junction string in parallel with a higher I_C Josephson Junction string with an upper common connection connected to the output terminal and a pulsed DC current source. A ten-stage Suzuki stack amplifier was shown by [12] to have a bandwidth of up to 10 GHz. The higher bandwidth of the Suzuki stack amplifier, made it the preferred SCE amplifier.

The Suzuki stack amplifier was designed in WRSPICE and a circuit layout was done in Lasi 6. The Hypres design rules were followed and a Monte Carlo analysis was done with Hypres manufacturing tolerances included. A DC-to-SFQ converter followed by a 250 μA JTL was used to generated the RSFQ pulses.

The Suzuki stack amplifier consisted of four lower I_C Josephson Junctions with $I_C = 450\mu A$ and four higher I_C Josephson Junctions with $I_C = 1mA$. The amplifier was synchronised by an external clock signal with a frequency of 3.33 GHz that can be increased up to 7 GHz. The amplifier had a rise time of 33 ps and a fall time of 31 ps. The peak voltage of the amplifier was increased from 160 μA up to 8.2 mA and the peak current was increased from 160 μA to 430 μA.

The Monte Carlo analysis showed a success rate of 89.8 %. However, the success of the circuit is mainly connected to the current received from the external clock signal and can be adjusted until the correct output is received. That will give the circuit a better success rate.

5.1.2 Commercially Available Amplifiers

Ten commercially available amplifier ICs were selected and tested in the cryorefrigerator at 4 K. Each amplifier was soldered on its own specifically designed PCB. A solid brass cover was used to connect the PCB to the cold finger of the cryorefrigerator. RF cable and SMA connectors were used to feed the input and output of the amplifier through the cryorefrigerator. The cable had a maximum specified frequency of 3 GHz [27]. Three of the ten

amplifiers worked down to 4 K.

The first amplifier was the HMC548 LNA. It comprises of two internally matched SiGe HBT amplifier stages. At room temperature, the HMC548 has a gain between 720 MHz and 1.9 GHz with a maximum gain of 19.5 dB at 1.2 GHz. When the amplifier was cooled down the 4 K, it showed a gain from 820 MHz to 1.9 GHz with a maximum gain of 20 dB at 1.2 GHz.

The second amplifier was the HMC460 LNA. It comprises of a GaAs MMIC p-HEMT LNA. The amplifier IC was firstly soldered on a FR4 PCB and cooled down to 4 K. It showed a gain up to 1 GHz with a maximum gain of 15.6 dB at room temperature and at 4 K. Then the evaluation board for the HMC460 LNA was adjusted for cryogenic measurements. The amplifier showed a gain over the complete 6 GHz spectrum of the spectrum analyser with a maximum gain of 17 dB. When the amplifier was cooled down to 4 K, the gain increased with up to 1.5 dB.

At room temperatures, the HMC460 LNA showed a minimum NF on the evaluation board of 4 dB at 300 MHz. When the amplifier was cooled down to 4 K, the NF dropped with more then 2 dB to reach a minimum NF of 1.74 dB with a gain of 17.4 dB at 200 MHZ. The amplifier had a quiescent power of 292 mW at 4 K.

The third amplifier was the THS4304 SiGe BiCom-III operational amplifier. It was designed to have a non-inverting gain of 17 dB. The amplifier showed a gain up to 400 MHz at room temperatures, and a gain up to 475 MHz at 4 K. The NF of the amplifier dropped with more than 6 dB with a decrease in temperature. At 4 K, it reached a minimum NF of 12.8 dB at 300 MHz with a gain of 5.8 dB. The quiescent power of the amplifier decrease with 20 %, from $92mW$ at 300 K to $73.5mW$ at 4 K.

Both the Bi-Com-III process from Texas Instruments Inc (THS4304) and the p-HEMT process (HMC460) work down to 4 K. The HMC460 amplifier has a wider frequency range, with a significantly lower NF than the THS4304.

However, the THS4304 has a lower quiescent power allowing it to reach 4 K easier. The THS4304 cost only $2.35 each, while the HMC460 cost $78.27.

5.2 Improvements and Future Work

As mentioned through the thesis, the SCE was only simulated. The layout of the SCE can be fabricated and physically tested in the cryorefrigerator. Then the SCE can be matched to the selected amplifier IC. The complete experiment can be set-up to detect and amplify RSFQ signals inside the cryorefrigerator at 4 K. The signals can be amplified to have enough power to be detected by room temperature electronics outside the cryorefrigerator.

Further tests can be done on different commercially available amplifier ICs, to find a larger range of amplifiers that can work at 4 K. The cables and SMA connectors inside the cryorefrigerator can be adjusted for higher frequencies and better results.

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