Invited Paper

# High-Performance Focal Plane Arrays Based on the HAWAII-2RG/4RG and the SIDECAR ASIC

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## ABSTRACT

The HAWAII-2RG based focal plane arrays represent one the most advanced imaging sensor technologies for near-infrared and visible astronomy. Since its introduction a few years ago, the HAWAII-2RG has been selected for a large number of space and ground-based instruments, including the James Webb Space Telescope. In addition, the SIDECAR ASIC, a fully integrated FPA controller system-on-a-chip, has been matured and is now being implemented in many of the next generation instruments. As a result of the SIDECAR ASIC, the detector system becomes a fully digital unit that is superior to the conventional discrete focal plane electronics with respect to power consumption, mass, volume and noise immunity. This paper includes an introductory description of the HAWAII-2RG and the SIDECAR ASIC, and presents the latest test results. It also discusses the latest generation of astronomy FPAs: the HAWAII-4RG. This new multiplexer contains all of the HAWAII-2RG features, but provides 4 times as many pixels at a pixel pitch of 10µm. Preliminary HAWAII-4RG test data is presented.

**Keywords:** Focal Plane Array, HAWAII-2RG, HAWAII-4RG, SIDECAR ASIC, Focal Plane Electronics

## 1. INTRODUCTION

In the late 1990s, the development of a new generation of hybrid focal plane arrays (FPAs) for scientific applications was initiated at Rockwell Scientific's Imaging division (now Teledyne Imaging Sensors), with the focus on future instruments for ground and space-based astronomy. The concept of a hybrid FPA that is combining a CMOS-based readout integrated circuit (ROIC) with a photo diode detector array had been successfully applied to many image sensors before. The new FPAs were designed to take advantage of the recent improvements in CMOS technology and in detector technology to provide better performance, higher resolution and more functionality. Furthermore, the development included an improved solution for the control electronics: a single chip comprising clock generation, bias generation and analog-to-digital conversion, located in close proximity to the FPA.

Initially, two new ROICs were designed: the HAWAII-1RG and HAWAII-2RG. The acronym is short for HgCdTe Astronomy Wide Area Infrared Imager with Reference pixels and Guide mode. Both ROICs are based on the same improved architecture, but differ in their resolution of 1024 x 1024 pixels and 2048 x 2048 pixels, respectively. They can be hybridized to a variety of detector materials, including HgCdTe, InGaAs and Si, depending on the desired wavelength sensitivity. HAWAII-2RG-based FPAs with HgCdTe detector arrays have demonstrated very low dark current of $< 0.01$ e-/s while maintaining high QE and low read noise. They have been selected by the James Webb Space Telescope for integration into the three near-IR instruments, and by a number of ground-based observatories for the current or next generation instruments. Over the past couple of years, the HAWAII-4RG has joined the family of available ROICs, providing 4k x 4k resolution within a single FPA. Due to its reduced pixel pitch on 10µm, the HAWAII-4RG is better suited for visible applications, and first hybrids with Si-PIN diode arrays (HyViSI technology) have already been demonstrated.

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In parallel with the HAWAII-1RG/2RG ROICs, the SIDECAR ASIC was developed as a companion chip. The acronym SIDECAR stands for System for Image Digitization, Enhancement, Control and Retrieval, and it describes all the tasks carried out inside the chip. The SIDECAR ASIC replaces conventional focal plane electronics by providing the same or better functionality and performance at lower power and much less volume. Due to its large operating range from room temperature to cryogenic temperatures as low as 35 K, the SIDECAR ASIC can be placed in direct proximity of the FPA for almost any application, thus reducing signal integrity issues and power consumption. A number of next generation astronomical instruments are implementing the SIDECAR ASIC as the FPA controller for the HAWAII-2RG/4RG FPAs. An unexpected application for the SIDECAR has emerged with the unfortunate failure of the Advanced Camera for Surveys (ACS) on the Hubble Space Telescope. The repair mission for ACS will install new CCD drive electronics that includes the SIDECAR ASIC as the core component for control and digitization.

## 2. ROIC ARCHITECTURE

### 2.1. Description of the HAWAII-2RG

This section will give a brief overview of the HAWAII-2RG. A more detailed description can be found under Loose et al. [1]. Figure 1 shows the block diagram of the HAWAII-2RG. The main building blocks can be grouped into the pixel array, the vertical scanner, the horizontal scanner, the column buffers, the serial interface logic and the I/O pad structure. The pixel array consists of 2048 x 2048 pixels. Its outer 4 rows and columns on either side contain reference pixels, leaving a total of 2040 x 2040 pixels as active detector pixels. The 18 µm pixels are based on a source follower circuit for low power and low noise operation. In addition, the pixel circuit provides single pixel reset capability, a critical requirement for guide mode operation.

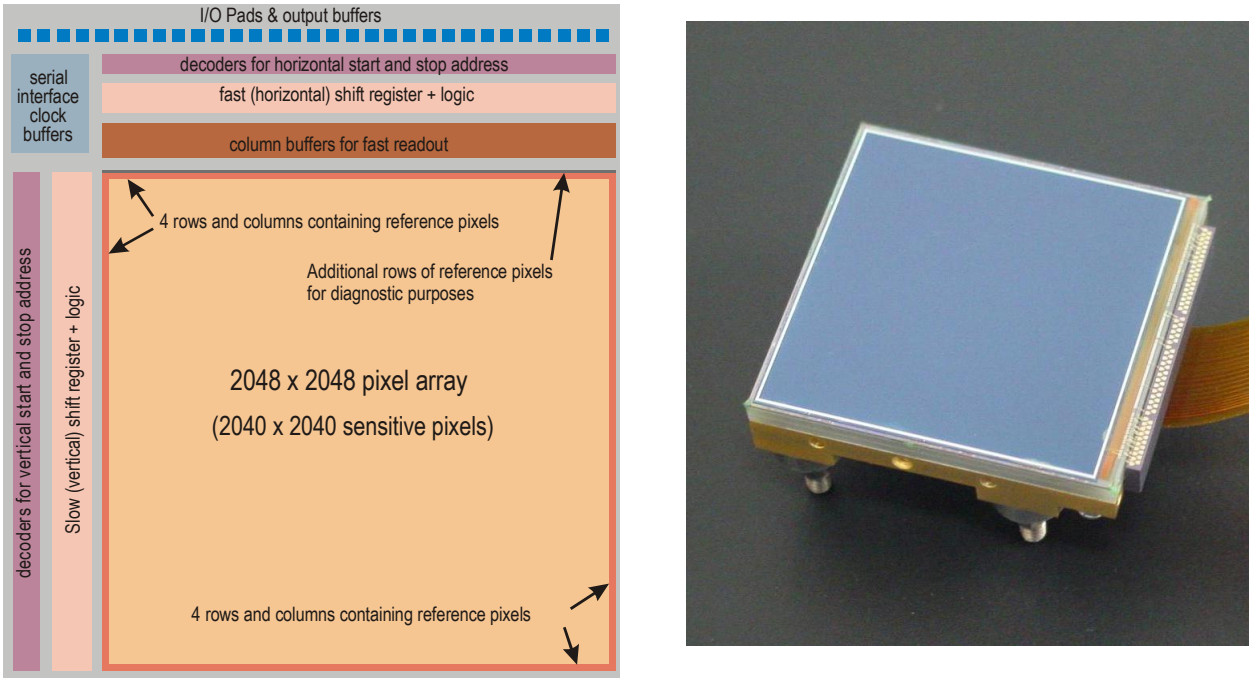



Figure 1: Block diagram (left) and photograph (right) of the HAWAII-2RG.

Depending on the required performance parameters such as frame rate, noise or power consumption, different output options can be selected. The HAWAII-2RG can be read out using a single output, 4 outputs, or 32 outputs. The pixel rate per output can reach up to 500 kpixels/s in slow mode and up to 10 Mpixels/s in fast mode, leading to a maximum frame rate of 4 frames/s in slow mode and 80 frames/s in fast mode. Optionally, the output signals can be buffered by an on-chip buffer stage to drive several meters of cable. However, lowest power is achieved by disabling the output buffer, and improved noise performance can be expected from shorter cables.

With earlier ROICs (e.g. HAWAII-1R), reference pixels demonstrated the capability of reducing low frequency noise on the bias voltages. Therefore, the concept of reference pixels has been maintained for the HAWAII-2RG, with improved functionality and performance. The embedded reference pixels in the array include a 40 fF capacitor to emulate the capacitance of the photo diode in the active pixels. The reference pixels are read out as part of the normal array and can be used during the data analysis phase for correcting bias variations. In addition, the HAWAII-2RG provides a separate reference output that can be monitored in real time. A typical use of this output is to connect it to the negative input of the preamplifier in the FPA electronics, resulting in a differential readout of the FPA. By this means, higher frequency noise components will be filtered out than with the embedded reference pixels.

A feature that had not been available on the older ROIC generation is the guide mode capability of the HAWAII-2RG. Guide mode refers to the simultaneous operation of a full field for science exposures and a sub-array for telescope guiding. The sub-array is thereby read out multiple times over the course of the full field readout to obtain a sub-array frame rate that is significantly higher than the full field frame rate. For a 10 x 10 pixel sub-array, the sub-array frame rate reaches 100 Hz when clocking at 200 kHz and allowing a 1% overhead in full field readout time (4 output mode). Many other window sizes and frame rates are possible, limited only by the pixel rate per output and some small clocking penalty for switching between sub-array mode and full field mode. For the sake of completion, it should be noted that the sub-array can also be operated without the simultaneous full field exposure. In that case, it is considered a normal window readout, and the frame rate can be calculated by dividing the pixel rate per output by the number of pixels in the window.

### 2.2. Description of the HAWAII-4RG

The development of the HAWAII-4RG is a direct continuation of the HAWAII-2RG design. All of the features have been maintained, and the operational concept is identical. However, due to opposing requirements for infrared and visible applications with respect to the pixel pitch, two separate approaches have been taken. The first design is the HAWAII-4RG-10, comprising an 4k x 4k array of 10 µm pixels. It is intended primarily for visible applications using a HyViSI silicon detector. The pixel design is a direct copy of the HAWAII-2RG source follower pixel, with the exception of the smaller geometry and an added protection diode. The second design is the HAWAII-4RG-15, which uses 15 µm pixels. The larger pixels are better suited for infrared applications, although visible detectors can be hybridized as well. Since the pixels provide extra space compared to the 10 µm pixels, more complicated pixel circuits are possible. At the time of the ROIC wafer production, one of three pixel options can be selected: source follower, capacitive trans-impedance amplifier, or direct injection. Several HAWAII-4RG-10 ROICs have been produced and hybridized to HyViSI detectors. The parts have been tested by several groups, and results are presented in Dorland et al. [2], Simms et al. [3] and in the test result section of this paper. As for the HAWAII-4RG-15, the design has been completed, but no actual ROICs have been built to date.

Figure 2 shows the block diagram of the HAWAII-4RG, and a photograph of a HAWAII-4RG-10 HyViSI hybrid FPA. It is quite apparent that the block diagram looks very similar to the HAWAII-2RG. The differences are mainly in the number of elements per block to accommodate the larger amount of pixels. Vertical scanner, horizontal scanner, and the column buffer array are matched to the 4k x 4k pixel matrix by containing 4096 elements each, twice as many as on the HAWAII-2RG. As before, the video outputs support both slow and fast readout mode, up to 500 kHz and up to 10 MHz, respectively. The output signals can be buffered for higher drive strength, or can be read out unbuffered for lower power and higher dynamic range. The HAWAII-4RG supports 1, 4, 16, 32, and 64 simultaneous output channels, with the 32 channel mode included specifically for single SIDECAR ASIC operation. Two SIDECAR ASICs have to be used to take advantage of all 64 output channels (only 36 ADC channels available per ASIC).

As in the HAWAII-2RG, the pixel array of the HAWAII-4RG is surrounded by 4 rows of reference pixels on all four sides. For improved compatibility with both silicon HyViSI detectors and HgCdTe infrared detectors, two types of reference pixel circuits can be selected. For HyViSI, the reference pixels will look just like regular active pixels and are in fact connected to real pixels on the detector. On the detector, however, the outer four pixel rows and columns are shielded such that no light can enter. Therefore, they behave as dark reference pixels. For the infrared FPAs, the reference pixels can be programmed to look like the traditional capacitor-based reference pixels known from the HAWAII-2RG. A separate permanent reference output for differential readout schemes is available as well, but unlike

before, the HAWAII-4RG derives the reference signal not from a single pixel, but from a full row of pixels. Various types of pixel circuits can be selected for this reference output, including the ones described above.

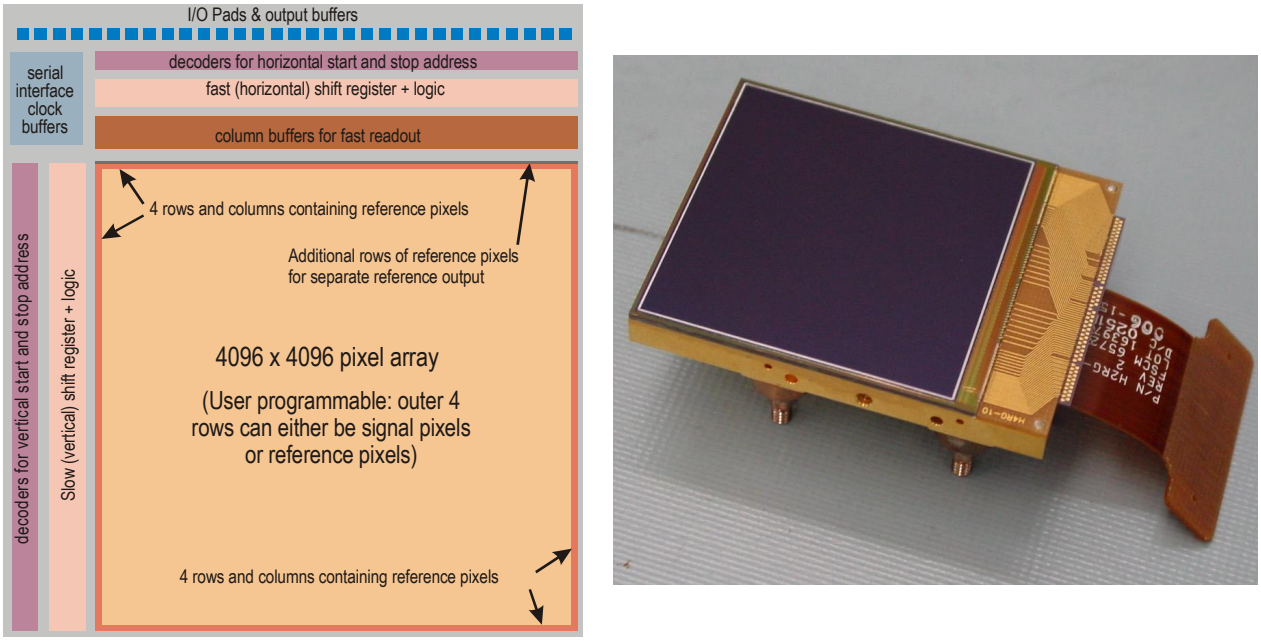



Figure 2: Block diagram (left) and photograph (right) of the HAWAII-4RG-10, hybridized to a HyViSI detector.

An interesting property of the HAWAII-4RG ROIC design is the fact that it can be stitched into multiple array sizes during the manufacturing process. For example, the same mask set can be used to build 4k x 4k, 6k x 6k or 8k x 8k devices. Even rectangular shapes like 4k x 2k or 6k x 2k are possible. A comparison between the HAWAII-1RG, HAWAII-2RG and HAWAII-4RG can be found in Table 1.

Table 1: Comparison between the different members of the HAWAII-RG family

| **Parameter** | **HAWAII-1RG** | **HAWAII-2RG** | **HAWAII-4RG** |
|---|---|---|---|
| Technology | 0.25 µm CMOS | 0.25 µm CMOS | 0.25 µm CMOS |
| Detector material | HgCdTe, Silicon PIN | HgCdTe, Silicon PIN | HgCdTe (only 15µm pixels), Silicon PIN |
| Output channels | 1, 2, 16 | 1, 4, 32 | 1, 4, 16, 32, 64 |
| Maximum pixel rate per output | 500 kHz (slow)<br>10 MHz (fast) | 500 kHz (slow)<br>10 MHz (fast) | 500 kHz (slow)<br>10 MHz (fast) |
| Pixel circuit | source follower | source follower | source follower,<br>CTIA and DI available on 15 µm pixel |
| Array size | 1024 x 1024 | 2048 x 2048 | 4096 x 4096, other dimensions selectable during ROIC production |
| Pixel pitch | 18 µm | 18 µm | 10 µm and 15 µm |
| Reference pixels | capacitive | capacitive | capacitive and shielded visible |
| Sub-array mode | guide mode and normal window mode | guide mode and normal window mode | guide mode and normal window mode |
| Operating temperature | 30K – 300K (ROIC) | 30K – 300K (ROIC) | 30K – 300K (ROIC) |
| Read noise<br>(CDS, 30 < T < 120K) | < 15 e- (slow)<br>< 40 e- (fast) | < 15 e- (slow)<br>< 40 e- (fast) | < 10 e- (slow, source follower, HyViSI)<br>< 40 e- (fast, source follower, predicted) |
| Full well capacity | 100 – 150 ke- | 100 – 150 ke- | 100 – 150 ke- (source follower),<br>~1,000 ke- (CTIA), ~10,000 ke- (DI) |

## 3. SIDECAR ASIC DESCRIPTION

The SIDECAR ASIC was developed as a companion chip to the HAWAII-2RG ROICs and supports all of the possible FPA modes and configurations. At the same time, however, it was generically designed to be compatible with a wide variety of other image sensors and applications. All of its functions are fully programmable and can be adapted to the given requirements. The SIDECAR ASIC is optimized for use with analog CMOS-based detector arrays that require biases, clocks and power supplies in the range from 0 to 3.3V. Image sensors that require different voltages can be made compatible by means of additional discrete circuitry. The SIDECAR ASIC is designed to operate from room temperature all the way down to cryogenic temperatures as low as 30 K.

The left half of figure 3 shows a block diagram of a typical SIDECAR-driven detector system. The top block represents the FPA, which is connected to the SIDECAR (center block) via many analog and digital wires. At the bottom of the SIDECAR block, only digital wires go to the external data acquisition system. Due to the immunity of the digital signal transmission, which can be LVDS or LVCMOS, the acquisition system can be located several meters away from the SIDECAR ASIC. The basic SIDECAR architecture, as shown in the diagram, can be divided into the following major blocks: generic digital I/O, bias generator, A/D converter, digital control and timing generation (micro-controller), data and program memory, and digital data interface.

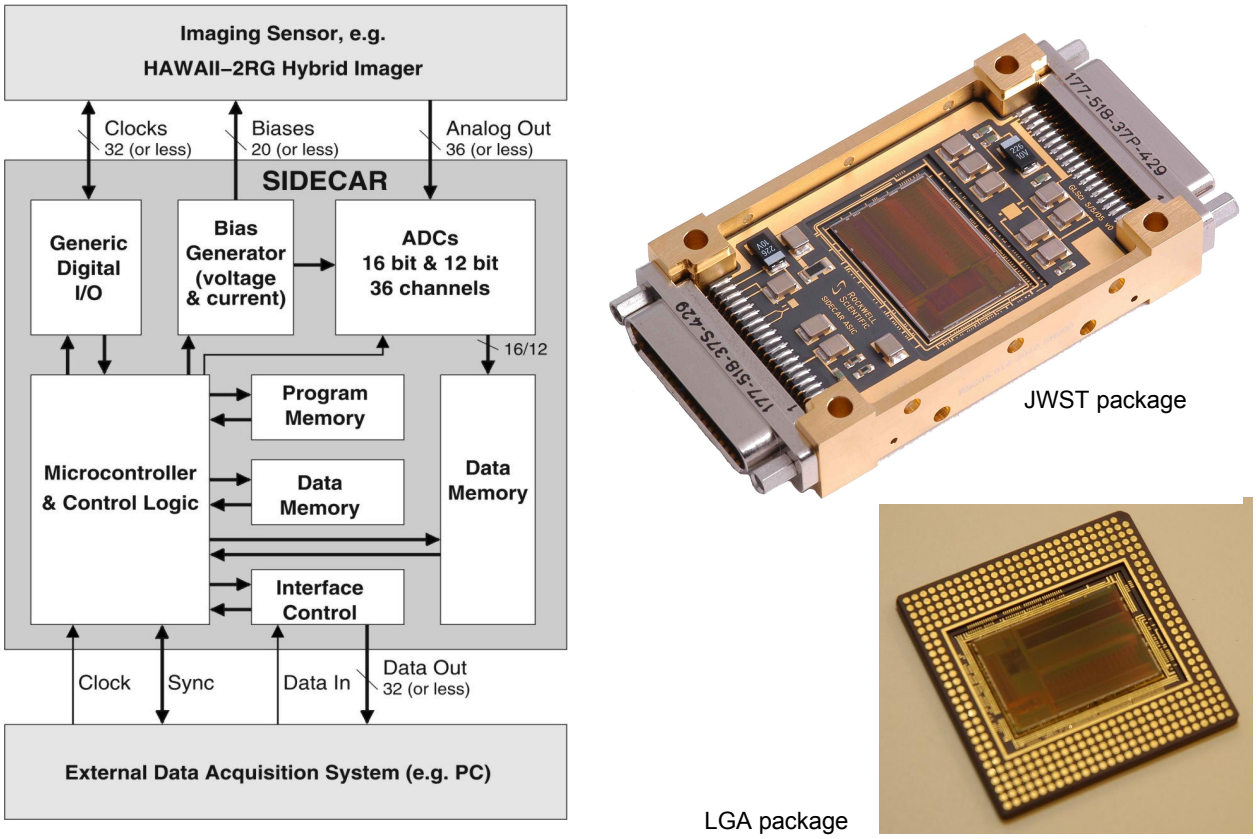



Figure 3: Block diagram (left) and two different packaging options (right) of the SIDECAR ASIC.

The analog bias generator consists of 20 independent channels, each of which is composed of a 10-bit digital-to-analog converter and an output buffer with adjustable driver strength. Each channel can be used as a programmable current

source from 0.1µA to 25mA and a programmable voltage source covering the range from 0V to 3.3V. For reading out the analog detector signals, the SIDECAR provides 36 analog input channels. Each channel can be digitized by on-chip ADCs offering 16-bit resolution at sample rates up to 500 kHz and 12-bit resolution at sample rates up to 10 MHz.

A fully programmable and application optimized micro-controller is responsible for the overall SIDECAR control and for generating the specific timing patterns of the image sensor clocks. A total of 32 digital I/O channels can be individually adjusted for driver strength and signal direction. Additional on-chip memory linked to an array processor with 36 channels permits simple data processing functions like pixel averaging or data sorting. Finally, serial and parallel data interfaces are implemented to read the digitized pixel values and to program the ASIC. The data interface can be operated at speeds up to 80 Mbits per line in single data rate mode (one bit per clock cycle) with a maximum bus width of 24 signals. Therefore, the maximum data bandwidth is about 1.9 Gbit/s and corresponds to 32 analog detector channels digitized at 5 MHz with 12 bit resolution. Table 1 summarizes the main SIDECAR ASIC properties.

Table 2: Summary of the SIDECAR ASIC properties

| | |
|---|---|
| Die Dimension | 22 x 14.5 mm² |
| Technology | 0.25 µm CMOS |
| Analog Input | 36 independent channels, fully differential |
| Preamplifiers | Programmable gain (-3 to 27 dB) and bandwidth |
| 16 bit ADCs | Up to 500 kHz sample rate (1 mW / channel at 100 kHz) |
| 12 bit ADCs | Up to 10 MHz sample rate (10 mW / channel at 5 MHz) |
| Bias Outputs | 20 output channels, selectable voltage or current DACs |
| Digital I/O | 24 channels (CMOS), 16 channels (LVDS) fully programmable |
| Micro-controller | 16 bit RISC, low power, excellent arithmetic capabilities |
| Program Memory | 16 kwords (16 bit / word) |
| Data Memory (µC) | 8 kwords (16 bit / word) |
| Data Memory (ADC) | 36 kwords (24 bit / word) |
| Array-processor | Adding & multiplying and DMA control per ADC channel |
| Digital Interface | LVDS or CMOS, custom serial protocol, up to 32 parallel lines |
| Operating Temperature range | 30 K – 300 K |
| Radiation | Complete design is single event upset protected |

Several packaging concepts have been designed for the SIDECAR ASIC. The right side of figure 3 depicts two of the most frequently used packages. The top photograph shows the JWST flight package, developed specifically for the James Webb Space Telescope to fit into the cryogenic environment of the near-infrared instruments. The ASIC die is mounted and wire-bonded on a ceramic carrier to guarantee good thermal conduction. The package also includes all filter and bypass capacitors needed for lower noise operation. On either end of the ceramic board, a 37-pin micro-D connector links the external cables to the corresponding signals of the SIDECAR ASIC. One connector handles the mixed-mode interface to the HAWAII-2RG detector and includes clocks, bias voltages and 6 analog input channels. The other connector provides access to the digital interface and the power supplies. It also includes the signals for the on-board temperature sensor and the optional heater resistors. The metal enclosure provides electrical as well as optical shielding and protects the SIDECAR die against mechanical damage.

The package shown on the bottom right of figure 3 is an LGA ceramic package designed for board level mounting. It is being used by all ground-based SIDECAR applications, and has demonstrated compatibility with room temperature and cryogenic operation. A hermitically sealed derivative of this package has been developed for use on the Hubble Space Telescope and is currently being qualified for flight application.

## 4. MEASUREMENT RESULTS

### 4.1. SIDECAR ASIC Test Results

Over the course of the last few years, the SIDECAR ASIC has been thoroughly tested under different conditions. Overall cryogenic and room temperature performance has been reported in Loose et al. [4] and Wong et al. [5]), while measurement results specific to JWST can be found in Loose et al. [12]. The essential noise, linearity and power numbers obtained from these measurements are listed in table 4. The SIDECAR ASIC has achieved NASA Technology Readiness Level 6 (TRL6) status by January of 2007.

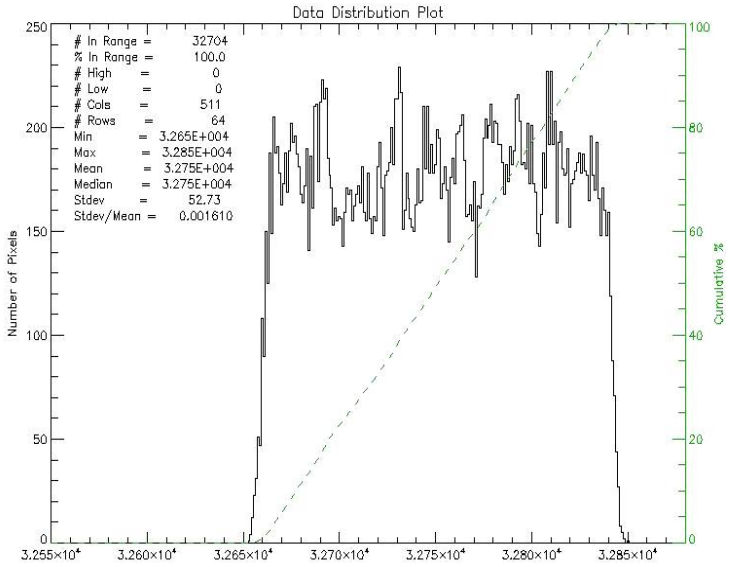
Table 3. Analog performance and power consumption in a JWST-like configuration

| Parameter | Measurement Result |
|---|---|
| Preamplifier noise at T = 37K | 12 μV (input referred at 27 dB Gain) |
| 12-bit ADC linearity | DNL < ± 0.3 LSB, INL < ± 0.8 LSB |
| 16-bit ADC linearity | DNL < ± 0.4 LSB, INL < ± 2.3 LSB |
| Power consumption | < 10.5 mW (4 ADCs, 100 kHz sample rate) |

Although the SIDECAR ASIC is capable of exhibiting equally low noise at room temperature and cryogenically, it is important to adapt the operation of the pre-amplifier and the ADC to the given temperature domain. Otherwise, low noise at low temperature will not automatically translate to low noise at higher temperatures. This issue stems from the fact that the pre-amplifier employs a capacitive feedback for the gain selection. Capacitive feedback circuits exhibits a floating node at the input of the amplifier, and it is necessary to set the floating node to a known potential by use of a transistor switch. Inevitable leakage currents in the silicon cause the floating node to drift, with a time constant that depends highly on temperature. Cryogenically, leakage currents are so small that no effective drift over the time of typical exposures is observable, and it suffices to perform the capacitor reset once per frame. All of the previously measured and published results were obtained using this reset scheme.

At room temperature, the pre-amp drifts are already apparent after only a few milliseconds. Given the desire to use the SIDECAR ASIC under warm conditions, in particular with its implementation as the CCD controller in the Advanced Camera of Surveys on the Hubble Space Telescope, we have examined the SIDECAR ASIC noise performance if resetting the pre-amp capacitors more frequently. Resetting the pre-amp every row, for example, will avoid the effects of the offset drift. Unfortunately, this approach introduces kTC noise on the input and feedback capacitors, and additional changes to the pre-amp configuration have to be made to remove the kTC noise by means of an intrinsic correlated double sampling scheme. Figure 4 illustrates the performance for the 3 different cases of pre-amp room temperature operation, each measured with the pre-amp inputs shorted to ground and at 100 kHz ADC sampling rate. At the top, the reset is performed once per frame, and significant drift can be seen. The middle image shows the case where the pre-amp capacitors are reset once per row. The noise histogram is largely reduced, but strong row-to-row noise stands out, caused by kTC noise in the capacitor feedback network. The bottom part finally demonstrates the proper configuration, which consists of a row-by-row reset combined with the kTC noise cancellation scheme. In that mode, the SIDECAR ASIC performs as expected, with an ADC dominated noise of about 2.6 ADUs or 32 μV (pre-amp gain of 4 selected).

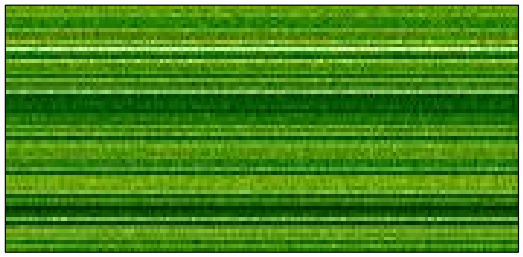
Using the kTC cancellation scheme, the dependence of the noise magnitude on the selected pre-amp gain has been examined. The results are plotted in figure 5, again measured with the pre-amp inputs shorted to ground. The left picture shows the output noise in ADUs as a function of gain, the right one shows the input referred noise in μV. The numbers represent the total SIDECAR ASIC noise including pre-amp, 16-bit ADC (running at 100 kHz) and any crosstalk contribution from the digital integrated circuits. Up to a gain of 4, the output noise is more or less constant around 2.7 ADU. This indicates that the noise is dominated by the ADC. When the gain is increased beyond 4, the output noise increases as well and identifies the pre-amp as the dominant noise source in this regime. Referring the measured noise back to input (right curve) shows that the ADC noise is about 160 μV (gain of 1), and that the pre-amp noise is about 12 μV (gain of 22). That latter value is obtained by subtracting the ADC noise in quadrature from the combined pre-amp and ADC noise of 14 μV at the highest gain setting of 22.

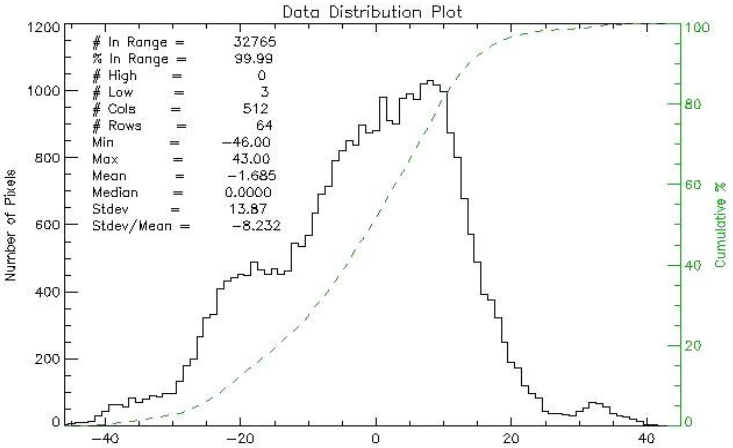



Pre-amp reset once per frame.

Noise (RMS): **52.7 ADU (650 µV)**

At room temperature, noise is dominated by pre-amp drift.

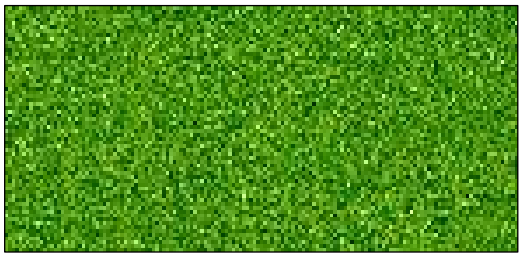


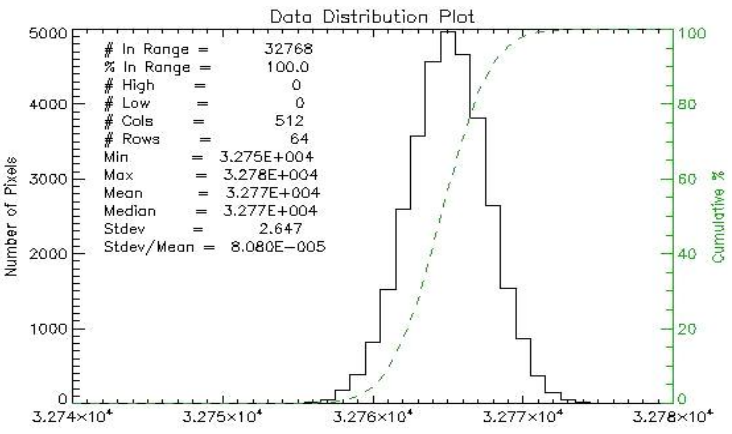



Pre-amp reset once per row.

Noise (RMS): **13.9 ADU (170 µV)**

Noise is dominated by row-to-row offsets, caused by kTC noise on pre-amp input capacitor.






Pre-amp reset once per row with kTC noise removal.

Noise (RMS): **2.65 ADU (32 µV)**

Noise is dominated by ADC noise (130 µV) input referred by the pre-amp gain of 4..

Figure 4: SIDECAR ASIC noise performance at room temperature, using different reset schemes from top to bottom.

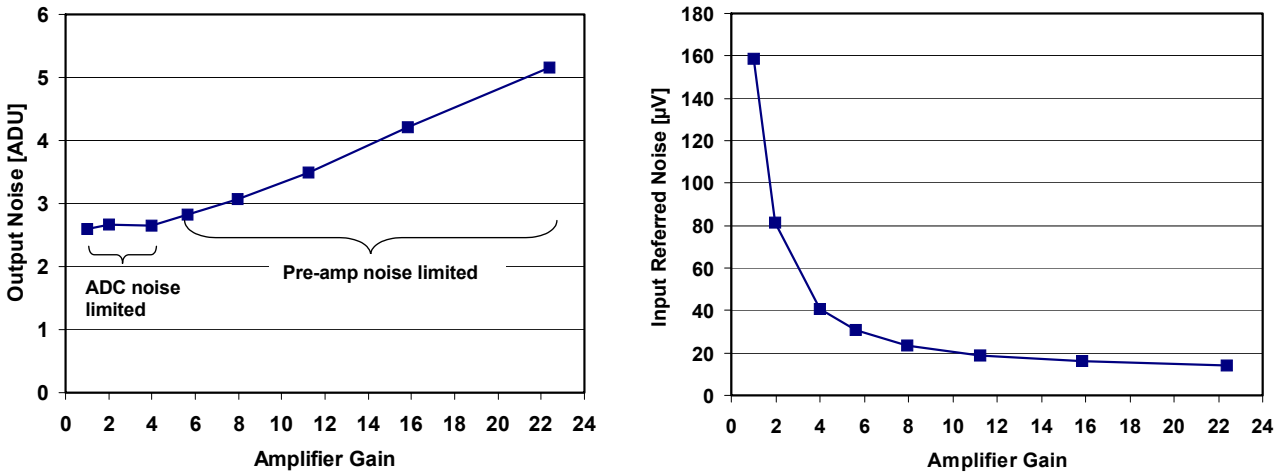



Figure 5: SIDECAR ASIC noise performance as a function of selected pre-amp gain. The left diagram shows the output noise in ADU, the right diagram shows the input referred noise in µV.

A useful property of the SIDECAR ASIC is its capability of reducing the digitization noise by averaging multiple ADC channels. The on-chip array processors can automatically co-add the digitized values from different ADCs, and then divide the final value by the number of co-added channels to obtain the average. In figure 6, the results from an experiment with up to 8 ADCs in parallel is shown. The input of the participating pre-amps were shorted to the same ground signal. The left side of the picture visually illustrates the reduction in noise by means of small pixel images displayed at the same scaling factor. The corresponding RMS noise numbers are plotted on the right as a function of number of averaged ADC channels. The reduction in noise follows the theoretical square root law almost perfectly, indicating uncorrelated noise contributions from each ADC. If an given application does not require all of the available SIDECAR ADC channels, this method represents a powerful tool to decrease the noise floor and thereby increase the dynamic range of the SIDECAR ASIC.

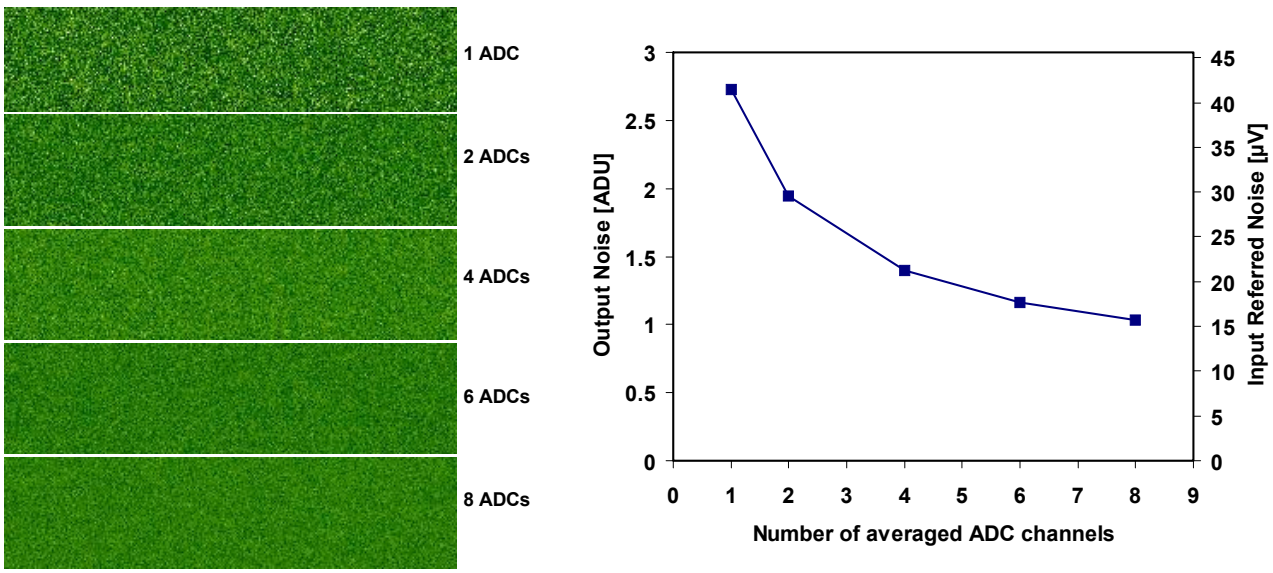



Figure 6: Reduction in SIDECAR ASIC noise by averaging multiple ADC channels.

In addition to the noise of the digitization chain (mostly pre-amp and ADC), the output noise of the bias generator plays an important role in the overall FPA performance. Figure 7 presents measurement results of the noise of a single bias outputs in voltage mode. The left side shows two 512 x 512 images, the top one acquired without any external filtering, the bottom one acquired using an external low-pass RC filter (time constant of 360 ms). The frame time per image was about 2s. The plot on the right shows the bias noise as a function of filter time constant. The total noise curve corresponds to the data as measured, the bias noise curve displays the same data if corrected for the pre-amp and ADC noise by subtracting their contribution in quadrature. The measurements were carried out using 4 ADCs in parallel (average scheme from previous paragraph) and the maximum pre-amp gain of 22 (27 dB).

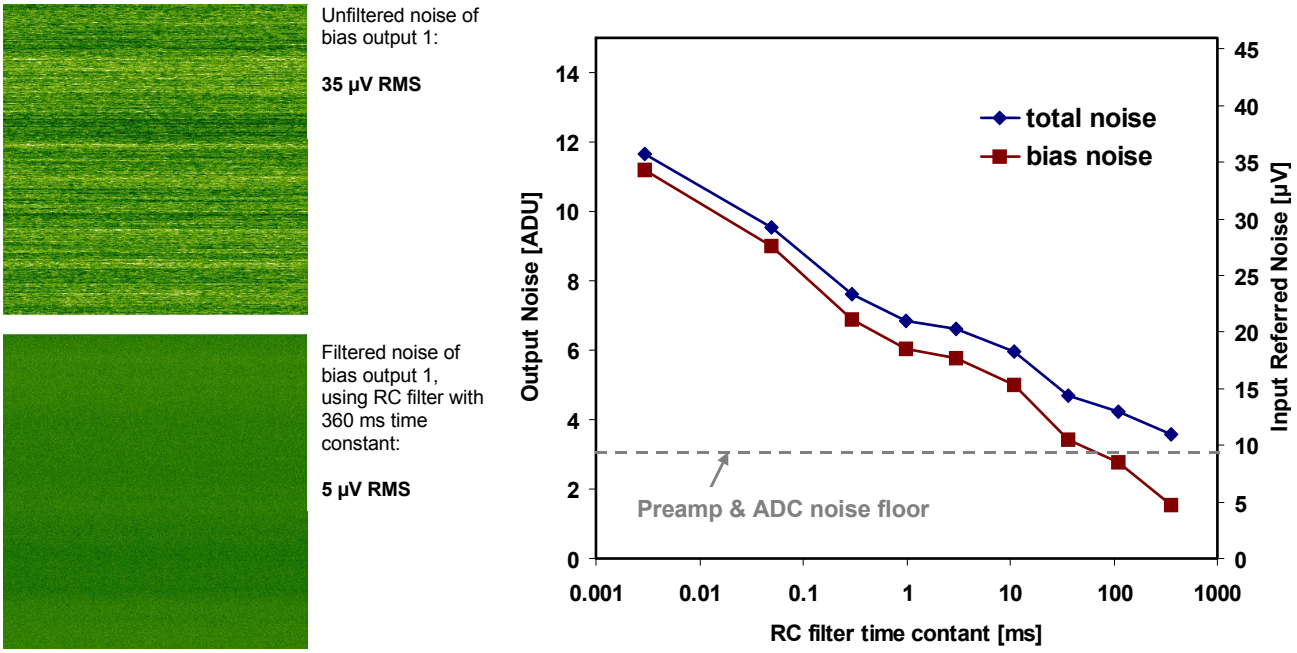



Figure 7: Measured output noise of the bias generator as a function of external low-pass filtering. Total noise includes the pre-amp and ADC component, bias noise is the extracted value when subtracting the pre-amp and ADC contribution in quadrature.

### 4.2. HAWAII-2RG Latest Results

The HAWAII-2RG has been in the hands of astronomy observatories and laboratories for a number of years, and numerous papers have been published. Performance results of infrared HgCdTe FPAs can be found in Finger et al. [6] and Waterson et al. [7], visible HyViSI detector results are reported in Bai et al. [8]. Other interesting data on guide operation and space based applications are discussed in Baril et al. [9], Riopel et al. [10], Rauscher et al. [11], and Loose et al. [12]. Most of the presented results have been measured using conventional control electronics. All data presented in this paper has been acquired using the SIDECAR ASIC. Since the electronics cannot affect dark current or quantum efficiency, only measurement results demonstrating correct functional behavior and achievable noise performance are included in the following. Furthermore, the focus is on fast mode noise results, which have not been reported before.

Figure 8 and figure 9 include measurements of an engineering grade HAWAII-2RG HgCdTe hybrid with 2.5 µm cutoff. The images were acquired at T = 37 K using the SIDECAR ASIC in a JWST flight package (16-bit ADCs at 100 kHz sample rate). The data is presented in ADUs with a conversion factor of 4.2µV/ADU. The typical conversion gain of a HgCdTe detector hybridized to a HAWAII-2RG and measured with the variance method (noise^2) is somewhere between 3 and 4µV/e-, sometimes even above 4µV/e-. Taking the effect of the inter-pixel capacitance (IPC) into account, the true conversion gain is about 20% higher (Finger et al. [13] and Moore et al. [14]). The actual conversion gain therefore spreads from about 3.6µV to over 4.8µV/e-, and the mid-level value is at 4.2µV/e-. In other words, the following plots can be directly interpreted in units of electrons rather than ADUs, with 1 ADU = 1 electron.

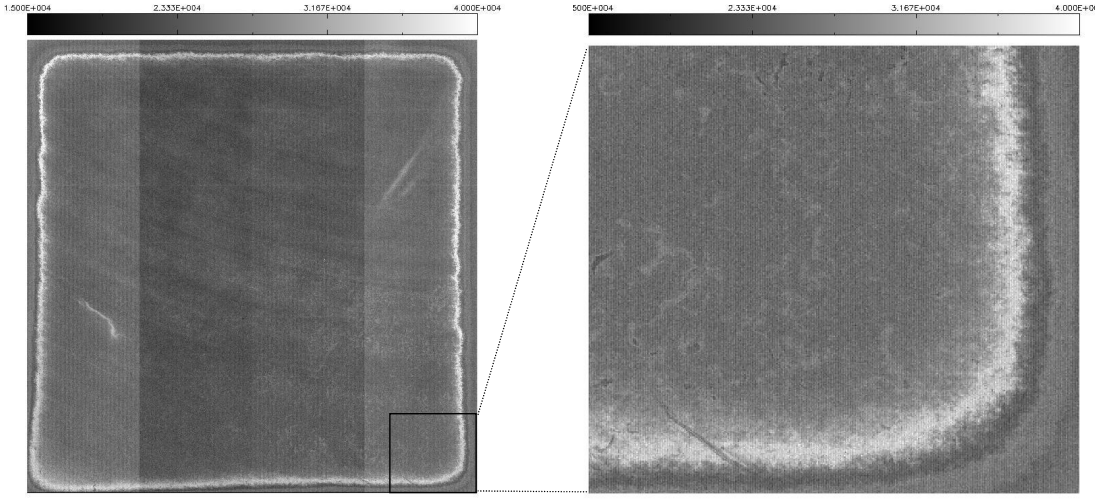


Figure 8: Image map and magnified cutout of a HAWAII-2RG hybrid with 2.5µm cutoff, controlled by the SIDECAR ASIC at 37K.

Figure 9 shows the noise results of a single CDS frame, calculated by looking at the standard deviation of each pixel through a set of 20 CDS frames. A median noise of about 21e- has been measured, which is typical for these types of engineering devices. Some detector defects are apparent in the upper left region, and higher noise is observed in the upper right field. The bright line in the middle from top to bottom is caused by incomplete settling of the first pixel and can be eliminated by allowing slightly more settling time at the beginning of a row.

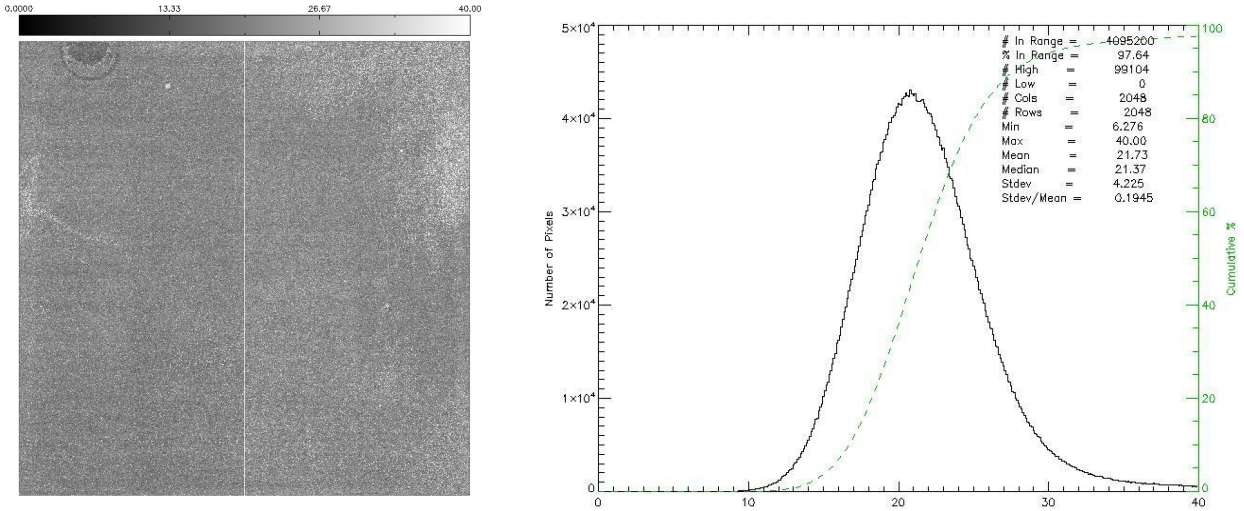



Figure 9: Noise map and histogram (single CDS) of a HAWAII-2RG hybrid with 2.5µm cutoff, controlled by the SIDECAR ASIC.

When configuring the HAWAII-2RG for fast mode with 32 outputs, and operating each output at 10 MHz, the frame rate amounts to 75 Hz. An example for fast mode is given in figure 10, which shows a HyViSI HAWAII-2RG image captured at 5 MHz speed using all 32 outputs. The reason for running at only ½ of the maximum speed is given by the limited data bandwidth of the SIDECAR ASIC (max. 160 Mpixels/s). The data is displayed in ADUs at 55 µV/ADU, and was acquired at T = 80 K. The CDS noise measured with the same setup is displayed in figure 11. The noise amounts to 2.68 ADUs, which equals 148 µV. If the typical IPC-corrected conversion gain for HyViSI pixels of 8 µV/e- is used, the CDS amounts to 18e-. When applying the same voltage noise to an infrared detector with a typical conversion gain around 4 µV/e-, the noise doubles to 36e-. Consequently, compared with the performance in slow mode (previous paragraph), fast mode provides 50 - 100 times faster frame rate at a noise level that is roughly doubled.

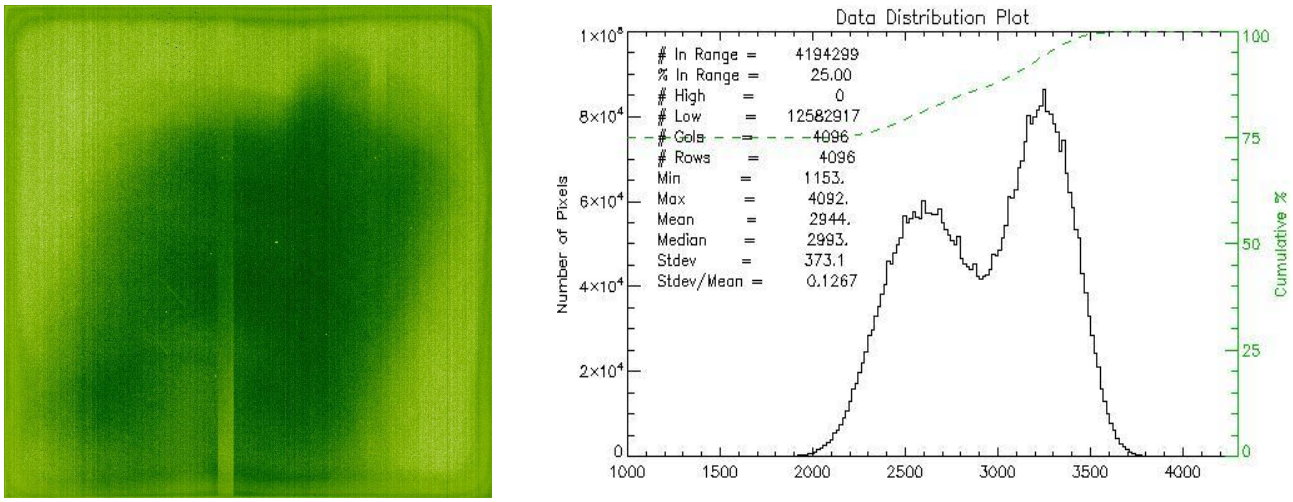



Figure 10: Image map and histogram of a HyViSI HAWAII-2RG operating in 32-output fast mode (5 MHz per output).

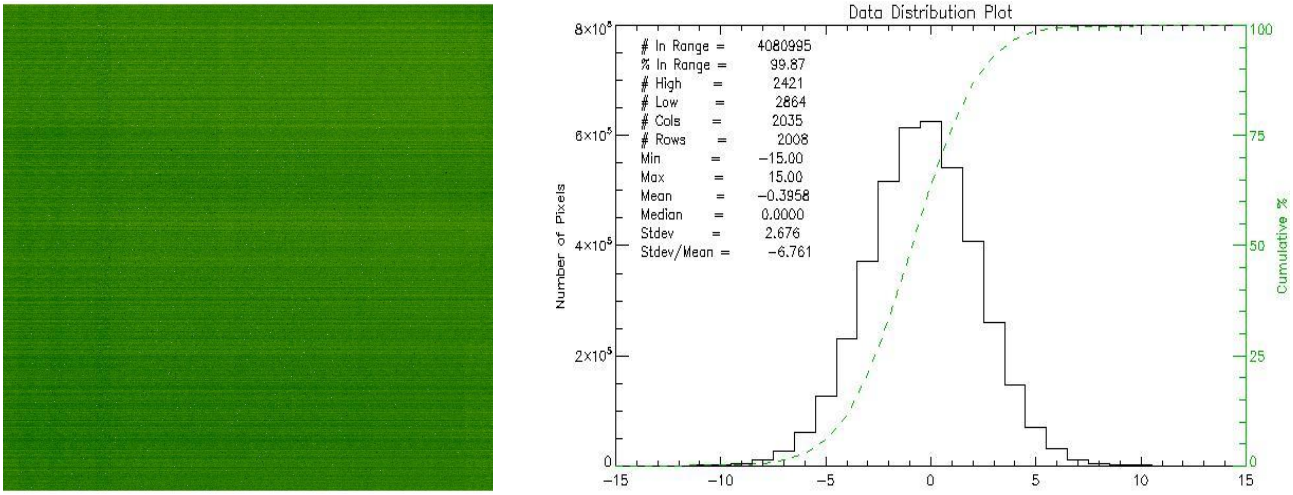



Figure 11: CDS noise map and corresponding histogram of a HyViSI HAWAII-2RG in 32-output fast mode (5 MHz per output).

### 4.3. HAWAII-4RG Preliminary Results

The first prototypes of HAWAII-4RG ROICs hybridized to a full 4k x 4k HyViSI detector array have been built and tested. The data is still preliminary, and especially dark current and noise will likely improve in the near future. The measurements were carried out at T = 173K, using 32 outputs in slow mode at 100 kHz. The SIDECAR ASIC was used as the FPA controller. Figure 12 contains the CDS noise results obtained from a set of 30 CDS frames. The noise is calculated individually for each pixel as the standard deviation through the 30 CDS frames. A conversion gain of 15 μV/e- was used, based on the simulated characteristics of a 10 μm pixel. The mean noise is 34e-, but contains some contribution from the dark current shot noise. Subtracting the dark current brings the CDS read noise closer to 30e-. The dark current map and the corresponding histogram are shown in figure 13. A circular pattern is quite apparent, a feature that is largely responsible for the relatively high dark current mean of 160 e-/s. It has been determined that the abnormally high dark current is caused by an anti-blooming diode in the multiplexer, which will be removed for the next revision. The HyViSI detector material itself exhibits normal behavior, including excellent quantum efficiency (similar to results formerly presented in Bai et al. [8]) and lower dark current. Lastly, the response map in figure 14 demonstrates high connectivity of more than 98.5%. The image was obtained by subtracting a dark image from an illuminated image, counting every pixel as connected that is above 50% of the array mean. The large non-uniformity in the response map is dominated by the non-uniformity of the illumination source.

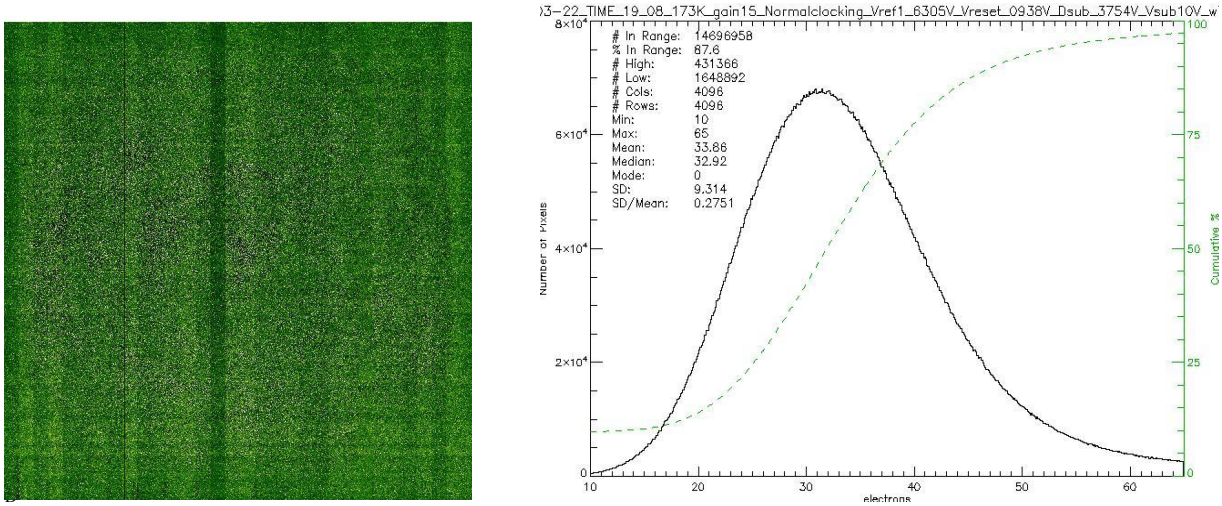



Figure 12: CDS noise map and histogram of a HyViSI HAWAII-4RG in 32-output slow mode (100 kHz per output).

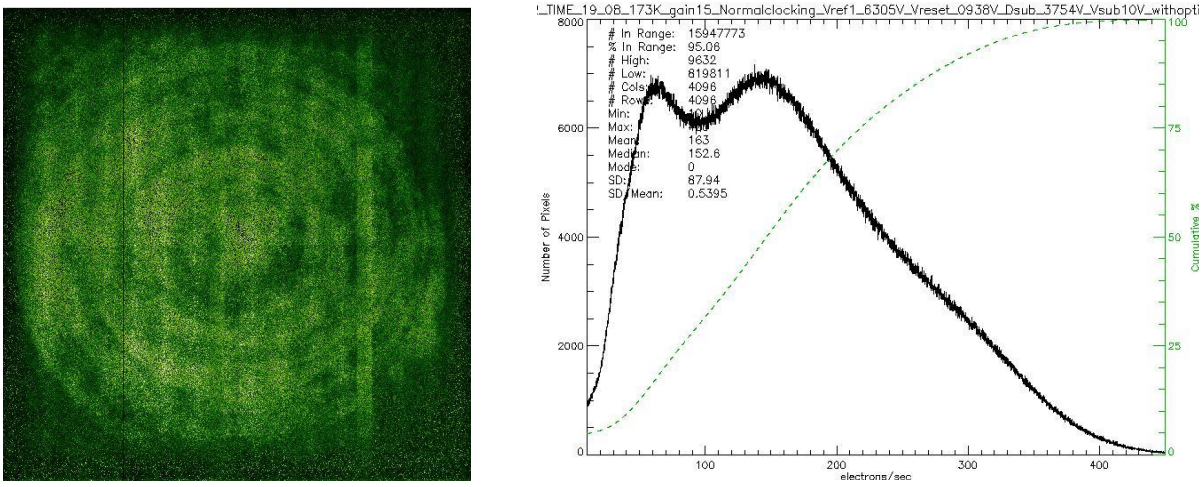



Figure 13: Dark current map and histogram of a HyViSI HAWAII-4RG, measured at T = 173K.

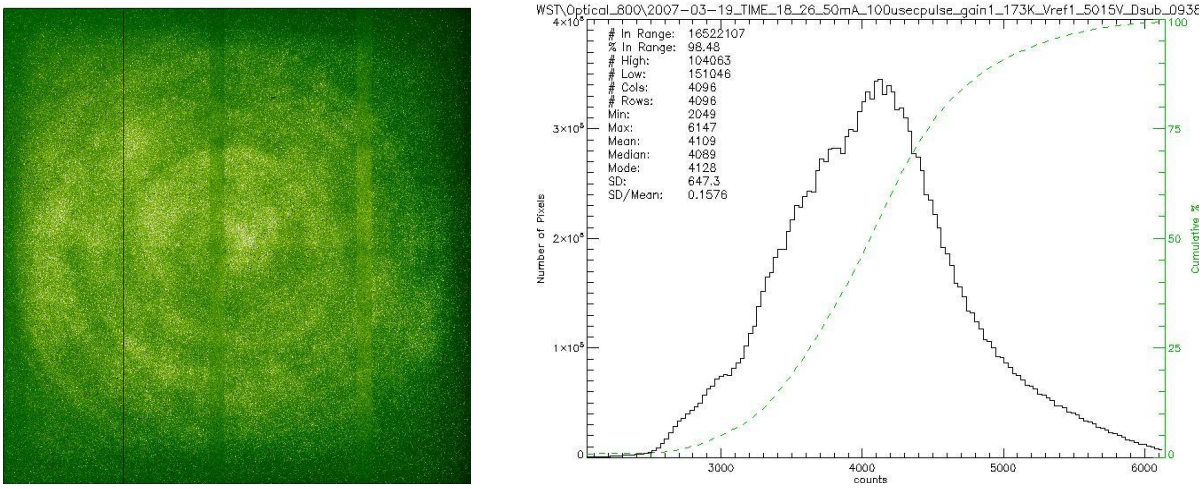



Figure 14: Response map and histogram of a HyViSI HAWAII-4RG, obtained by subtracting a dark frame from an illuminated frame.

## 5. SUMMARY

Driven by the need for a better detector technology for the next generation space telescopes, an advanced ROIC concept has been developed and successfully implemented. The HAWAII-1RG and -2RG based infrared FPAs have since become the preferred choice for many future ground-based and space based astronomy applications. In many cases, the detector is coupled with SIDECAR ASIC to provide a fully digital FPA solution. Impressive performance data has been collected by various groups, showing low noise, low dark current and near-100% quantum efficiency, both at slow and fast readout modes. More and more, the silicon-based HyViSI detectors are making inroads into the CCD dominated visible spectrum, offering advantages like electronic shutter, high red QE, radiation hardness, and operation under SIDECAR control. The latest addition to the ROIC family, the HAWAII-4RG, pushes towards smaller pixel sizes and higher resolutions while maintaining the high level of functionality and performance of its smaller siblings. Over the next decade, an essential role of the HAWAII-2RG/SIDECAR FPA technology in new astronomical discoveries can be expected.

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